Wideband Distributed Gain Block, DIE, 1.5 to 19 GHz

ENGDA00074

Typical Applications

- Military EW and SIGINT
- Obsolescence Replacement
- Receive or Transmit Circuits
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

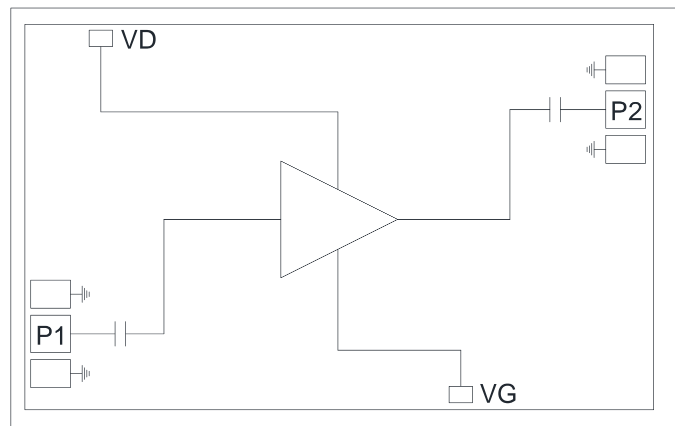
Features

- Wideband performance
- High Linearity
- 27 dBm IIP3, 35 dBm OIP3 at 9 V
- 34 dBm IIP2, 42 dBm OIP2 at 8 V
- 8-dB gain, positive gain slope
- Excellent return loss
  - 18 dB typical
- Size
  - 2.40 x 2.48 x 0.1 mm
  - 0.094 x 0.098 x 0.004 inch

Description

The ENGDA00074 is a wideband GaAs MMIC distributed amplifier die which operates from 1.5 to 19 GHz. The design is 50 ohm matched and includes on board bias circuitry. The amplifier offers 9 dB gain at 19 GHz with 1 dB of positive gain slope across the band. The amplifier is extremely linear with OIP3 near 15 dB better than OP1dB. The MMIC has gold backside metallization and is designed to be silver epoxy attached. The RF interconnects are designed to account for wire bonds and external microstrip flares for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



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Electrical Specifications, T = 25 ^{o}C, VD = 8.0 – 9.0 V; VG = -0.9 to -1.1 V

Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range	1.5 – 10.0			10.0 – 19.0			GHz
Gain	6.5	8.0		7	8.5		dB
Noise Figure		6			6		dB
Input Return Loss	14	18		15	20		dB
Output Return Loss	12	16		15	18		dB
Output P1dB	13	16		11 (@20 GHz)	16		dBm
Output IP3	31	35	(9 V bias)	31	35	(9 V bias)	dBm
Output IP2	38	42	(8 V bias)	38	42	(8 V bias)	dBm
Supply Current	160	195	240	160	195	240	mA
Thermal Resistance		40			40		^{o}C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD	7.5	8 - 9	10.5	V
ID		197		mA
VG	-0.8	-1.1	-1.4	V

Absolute Maximum Ratings

Parameter	Max level
Drain Voltage, VD	12 V
Gate Voltage, VG	-6 V
RF Input Power	+25 dBm
Channel Temperature	+165 ^{o}C
Operating Temperature	-55 ^{o}C to +100 ^{o}C
Storage Temperature	-65 ^{o}C to +150 ^{o}C

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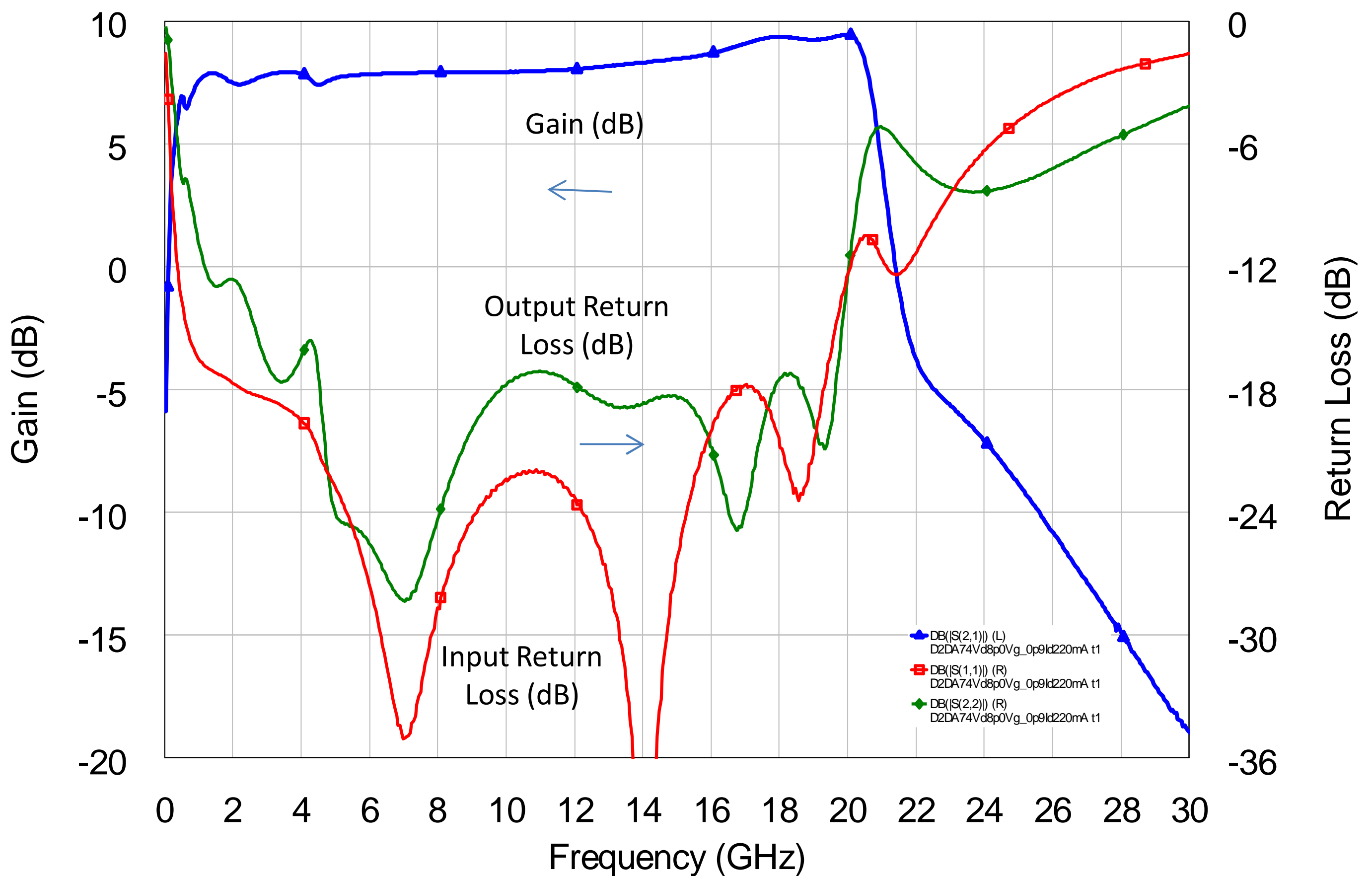
Measured RF Data with wirebonds & external microstrip flare pads

Gain and In /Out Return Loss (dB)

VD = 8.0 V; VG = -0.9 V ; ID = 222 mA



Measured RF Data with wirebonds & external microstrip flare pads

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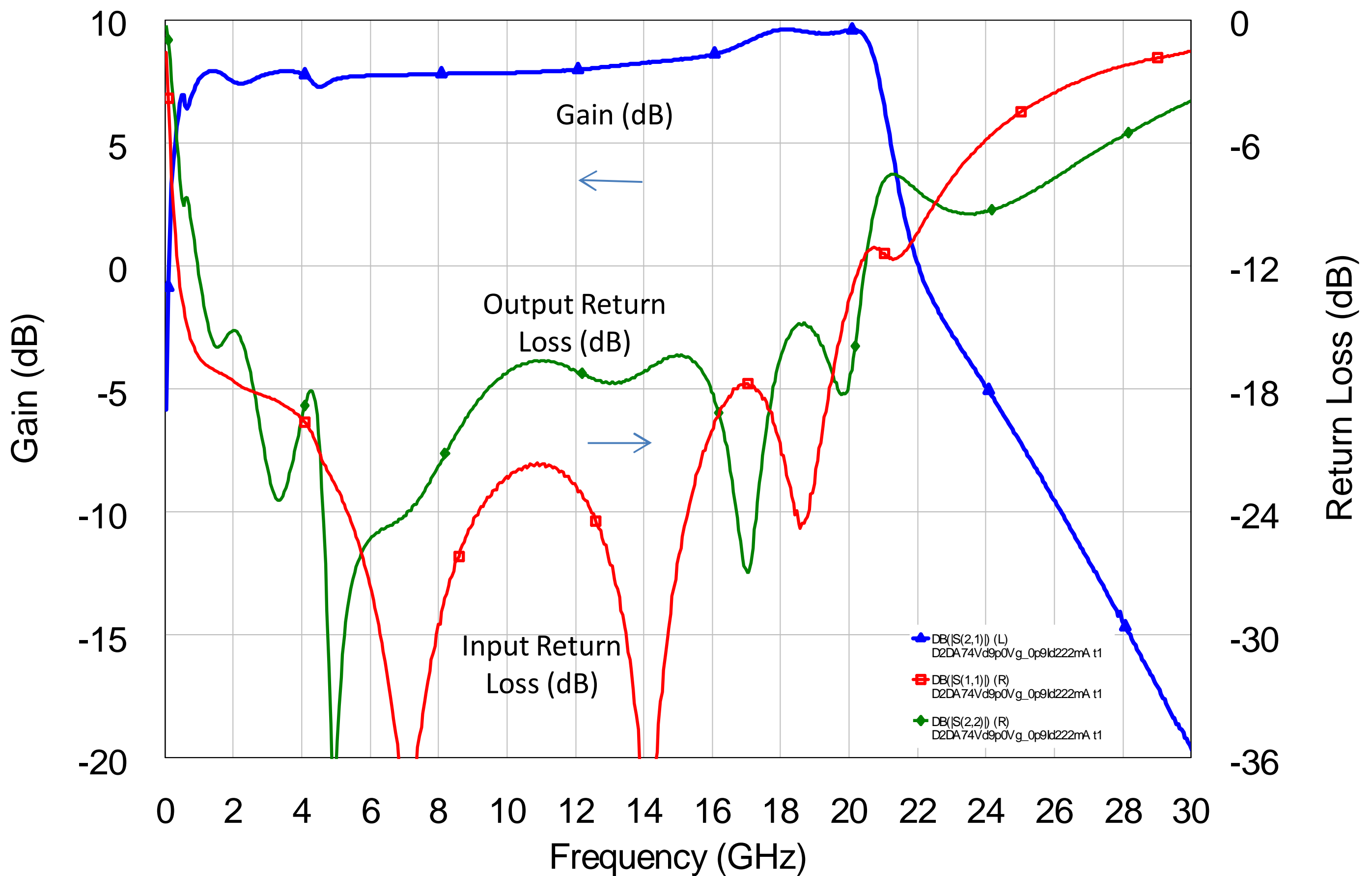

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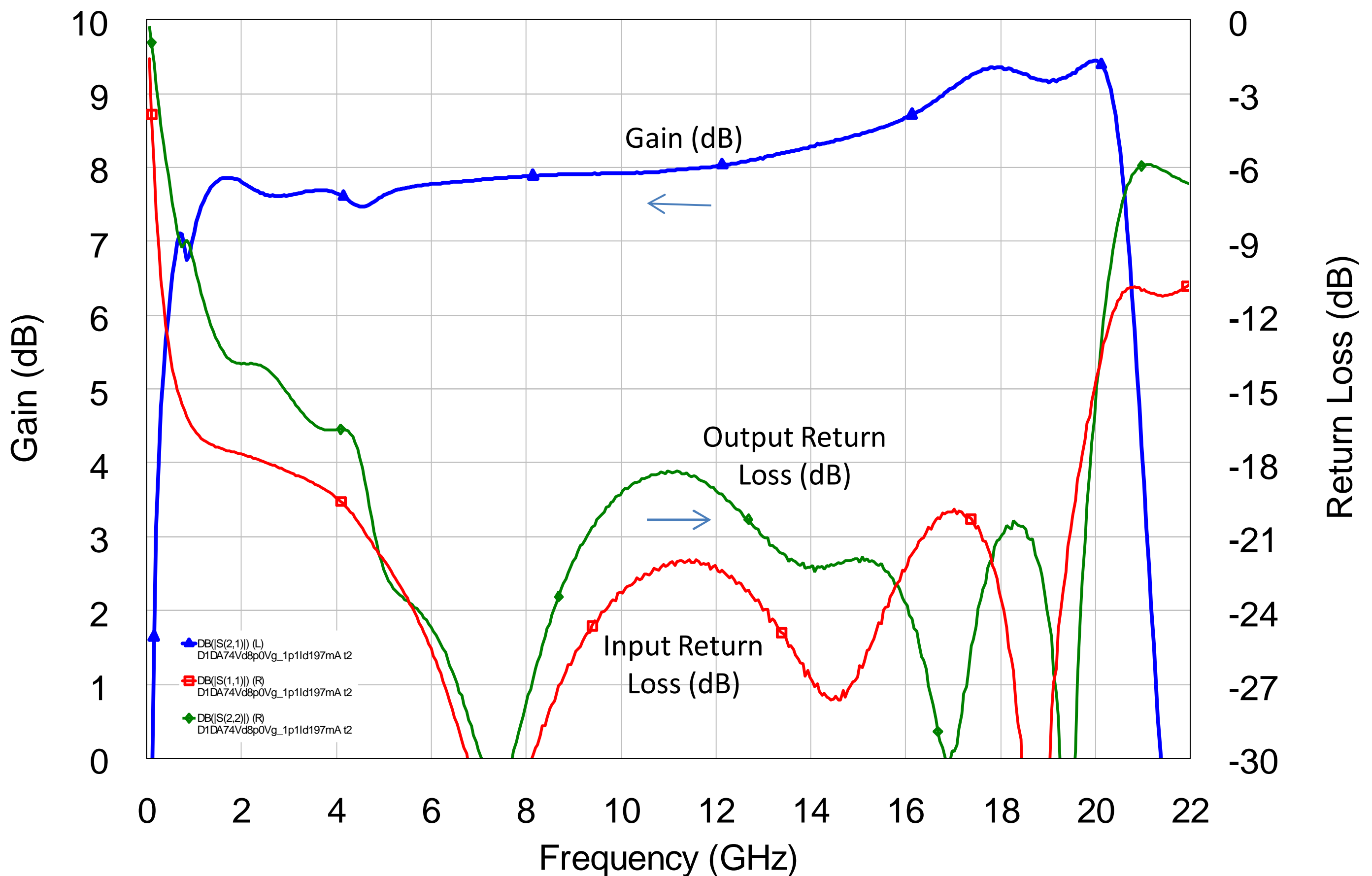

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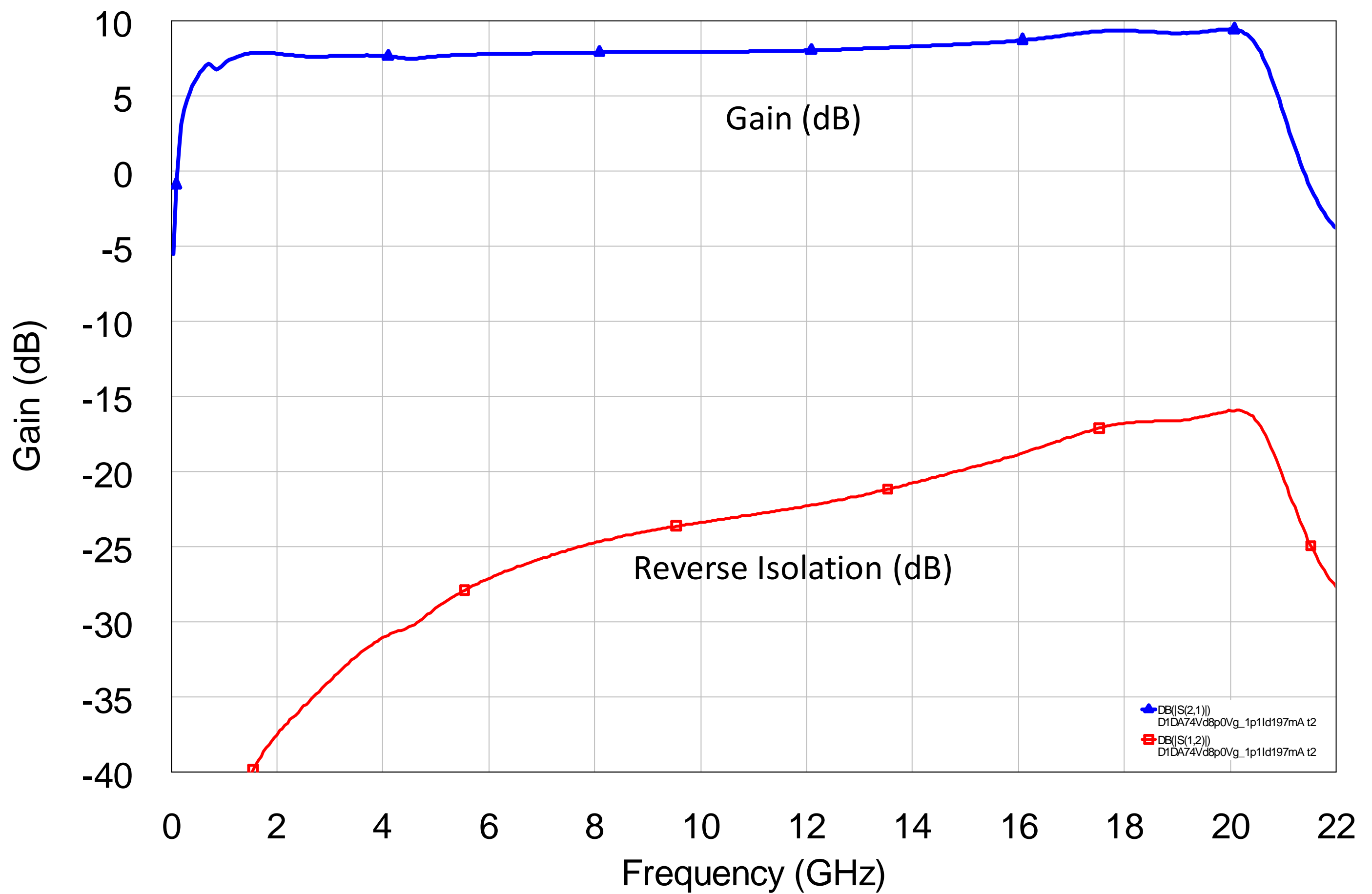
Measured RF Data with wirebonds & external microstrip flare pads

Gain and Reverse Isolation (dB)

VD = 8.0 V; VG = -1.1 V; ID = 197 mA



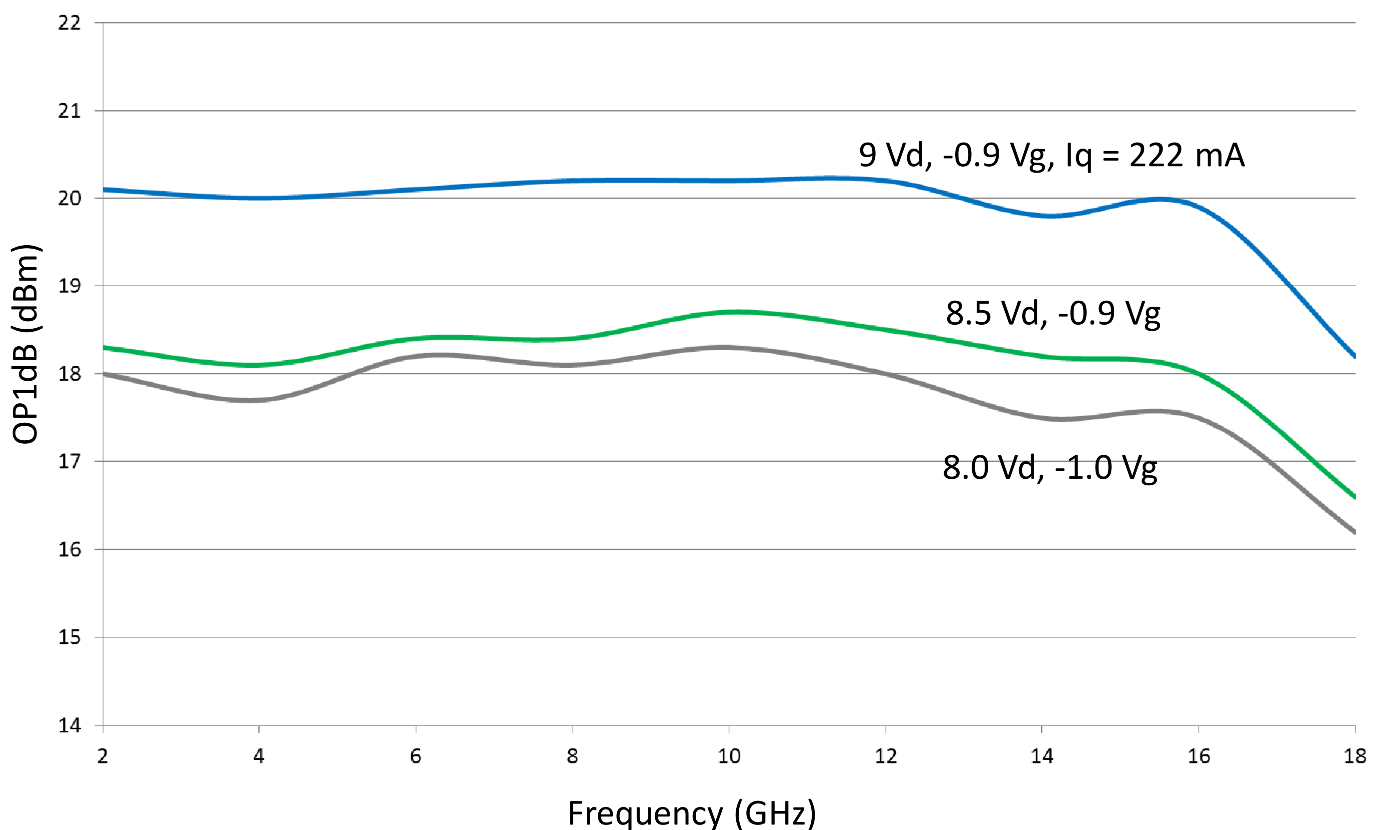
Measured Output Power at 1-dB Gain Compression (dBm)

VD = 8.0 to 9.0 V (optimum); VG = -0.9 or -1.0 V; room temperature

OP1dB = 20 dBm from 2 to 16 GHz at 9 Vd, -0.9 Vg

= 18 dBm from 2 to 16 GHz at 8 to 8.5 Vd, -0.9 to -1.0 Vg

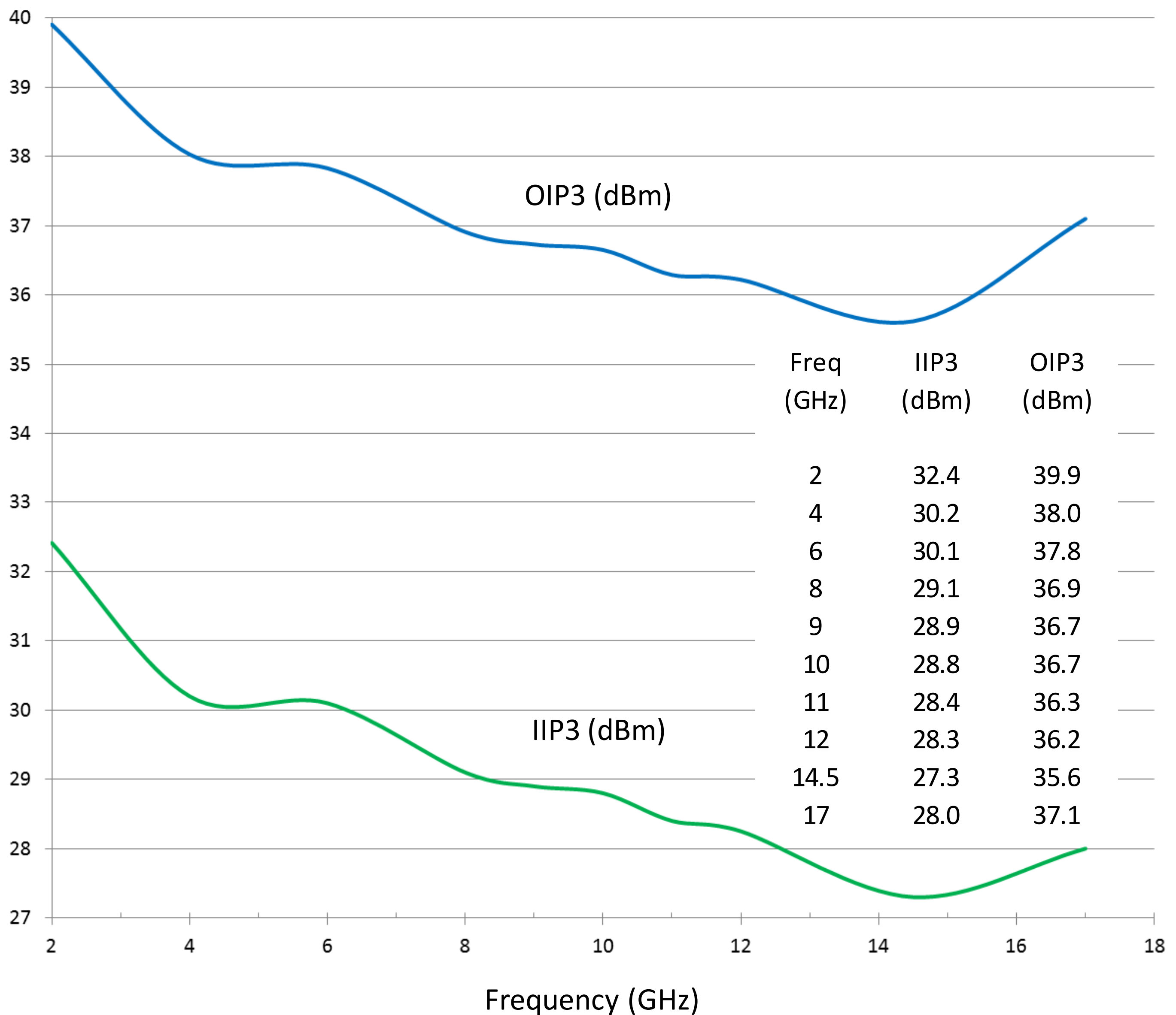
RF Data with wirebonds and external microstrip flare pads



Measured OIP3 > 35 dBm, IIP3 > 27 dBm, 2 – 17 GHz

VD = 9.0 V (optimum); VG = -0.9 V; ID = 222 mA; 0 dBm per tone (also measured same IIP3 and OIP3 performance at -10 and -5 dBm per tone)

RF Data with wirebonds and external microstrip flare pads



Freq (GHz)	IIP3 (dBm)	OIP3 (dBm)
2	32.4	39.9
4	30.2	38.0
6	30.1	37.8
8	29.1	36.9
9	28.9	36.7
10	28.8	36.7
11	28.4	36.3
12	28.3	36.2
14.5	27.3	35.6
17	28.0	37.1

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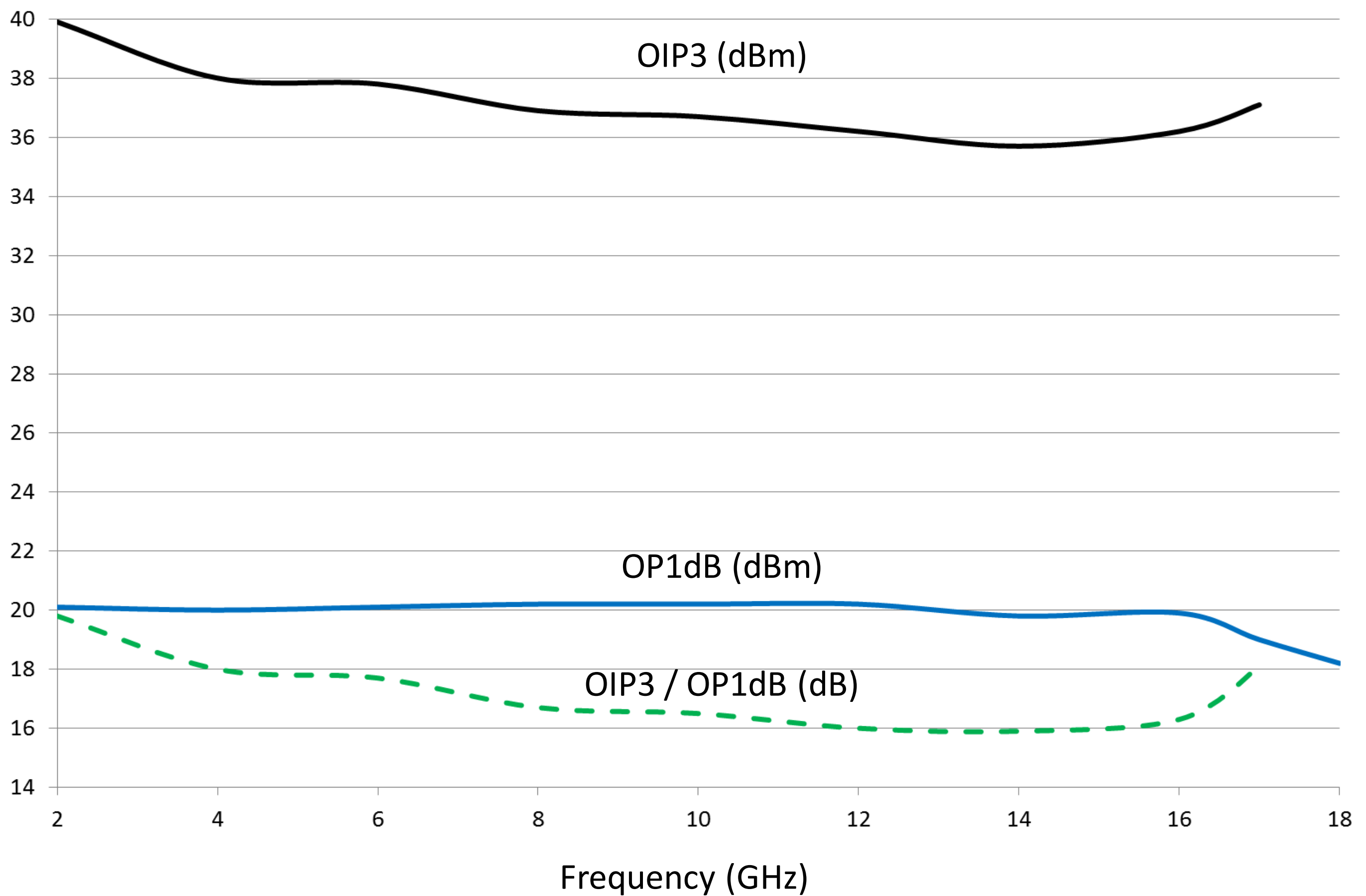
Measured Output Third-Order Intercept (OIP3, dBm) and Measured Output Power at 1-dB Gain Compression (OP1dB, dBm) & Ratio of OIP3 to OP1dB (dB)

VD = 9.0 V (optimum); VG = -0.9 V; Iq = 222 mA; room temperature



Measured IIP2 > 36 dBm, 8 V, -1.0 Vg (optimum bias for IIP2), 2 – 12 GHz

> 34 dBm, 8 V, -0.9 Vg; > 31 dBm, 9 V, -0.9 Vg

OIP2 ~ 8 dB higher than IIP2

Measured 2nd harmonic level (2 * F2) also provided

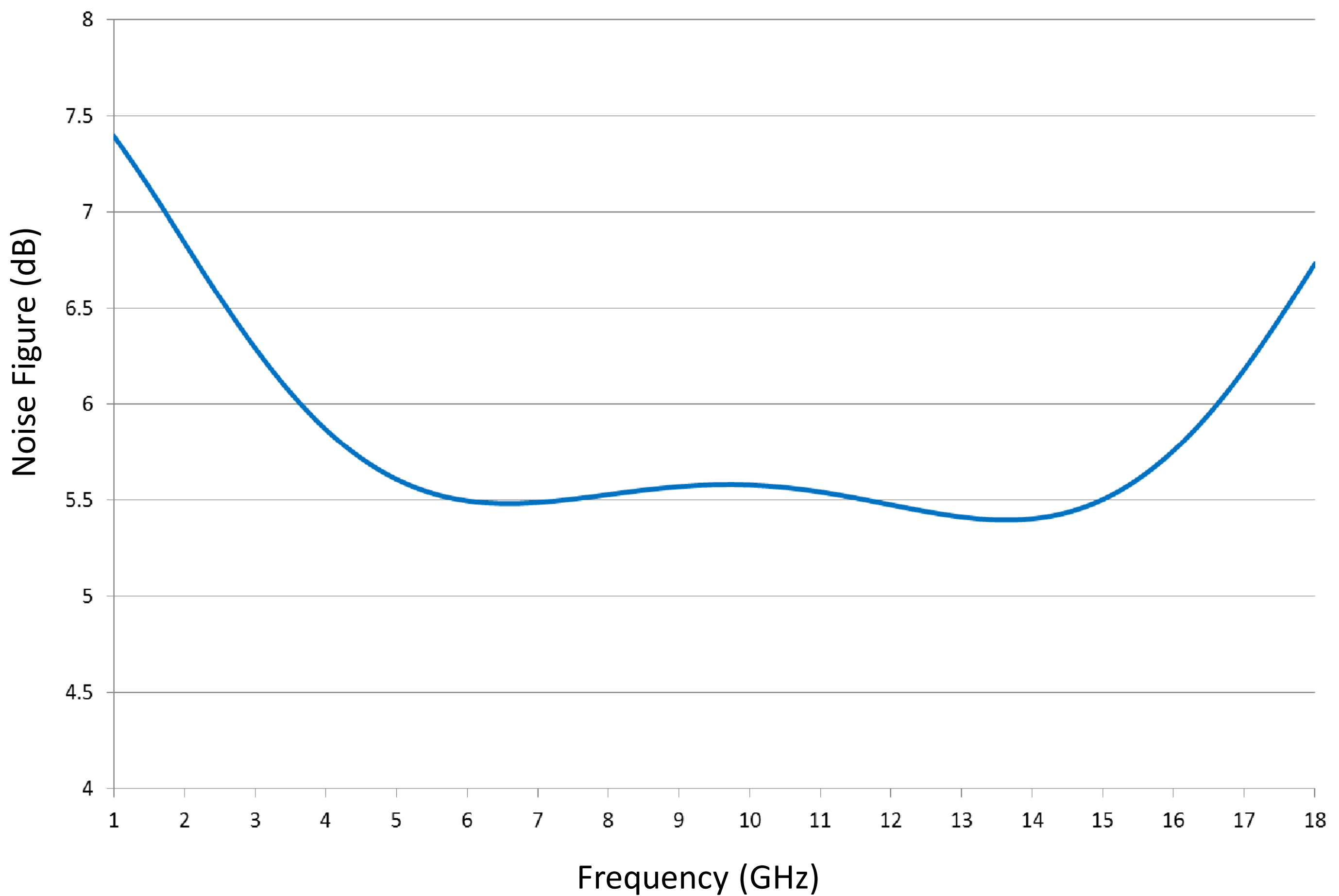
RF Data with wirebonds and external microstrip flare pads

Tone levels ranging from -5 to 0 dBm per tone; note frequency spacings

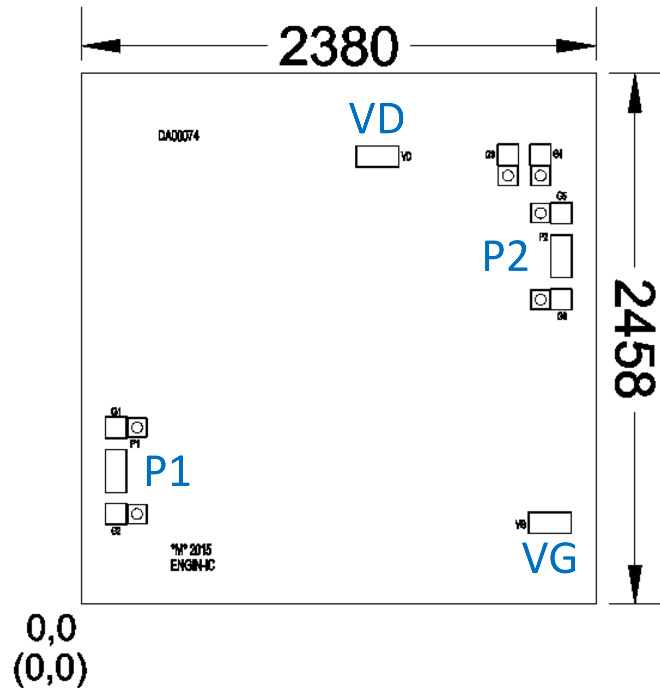
VD (V):	**8**	VG (V):	**-0.9**		VD (V):	**8**	VG (V):	**-1**		VD (V):	**9**	VG (V):	**-0.9**
F1	F2	IIP2	2*F2		F1	F2	IIP2	2*F2		F1	F2	IIP2	2*F2
(GHz)	(GHz)	(dBm)	(dBc)		(GHz)	(GHz)	(dBm)	(dBc)		(GHz)	(GHz)	(dBm)	(dBc)
		high side					high side					high side	
2	2.002	45.7	-52		2	2.002	44.5	-51		2	2.002	41.5	-48
4	4.002	38.7	-45		4	4.002	45.2	-51		4	4.002	35.2	-41
5	5.002	38.5	-45		5	5.002	44.8	-51		5	5.002	35.3	-41
8	8.002	34.2	-44		8	8.002	42.0	-48		8	8.002	32.7	-39
9	9.002	34.5	-41		9	9.002	41.2	-47		9	9.002	31.5	-38
10	10.002	38.0	-44		10	10.002	36.0	-42		10	10.002	31.3	-37
11	11.002	37.8	-44		11	11.002	38.0	-44		11	11.002	31.5	-38
12	12.002	43.5	-50		12	12.002	43.8	-50		12	12.002	33.8	-40
		low side					low side					low side	
		(2 GHz)					(2 GHz)					(2 GHz)	
8	10	42.5			8	10	49.2			8	10	47.2	
10	12	42.8			10	12	51.5			10	12	48.7	
12	14	37.5			12	14	45.2			12	14	48.2	
14	16	37.0			14	16	42.3			14	16	45.3	
16	18	33.5			16	18	38.2			16	18	48.2	

Measured Noise Figure, 1 to 18 GHz; 25 ^{o}C

VD = 8.0 to 9.0 V, VG = -0.9 to -1.0 V



Outline Drawing



	Pad Dimensions			
	Length (x-dim, um)	Width (y-dim, um)	Length (x-dim, mils)	Width (y-dim, mils)
P1 RF Input Pad Dimension	100	200	3.9	7.9
P2 RF Output Pad Dimensions	100	200	3.9	7.9
VD Drain Bias Pad Dimension	200	100	7.9	3.9
VG Gate Bias Pad Dimension	200	100	7.9	3.9

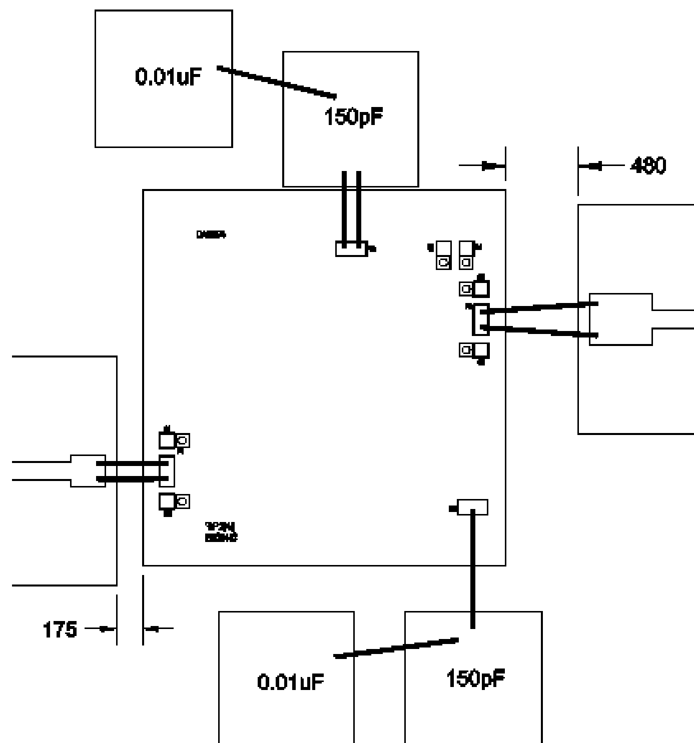
	RF Bond Pad Center Point Locations			
	x-dim, um	y-dim, um	x-dim, mils	y-dim, mils
P1 RF Input Pad Location	162	618	6.4	24.3
P2 RF Output Pad Location	2218	1611	87.3	63.4
VD Drain Bias Pad Location	1368	2073	53.9	81.6
VG Gate Bias Pad Location	2166	378	85.3	14.9

Notes:
1. ***All dimensions are given in both µm and mils. Substrate thickness: 100 µm (0.004”).***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

	RF I/O port - External Microstrip Flares on 5-mil Alumina				
	Flare Width y-dim, um	Flare Length x-dim, um	Wire Inductance (nH)	Wire Length (um)	Number of Wires
P1 RF Input Pad Flare Dimension	205	228	0.21	457	2
P2 RF Output Pad Flare Dimension	334	409	0.35	762	2



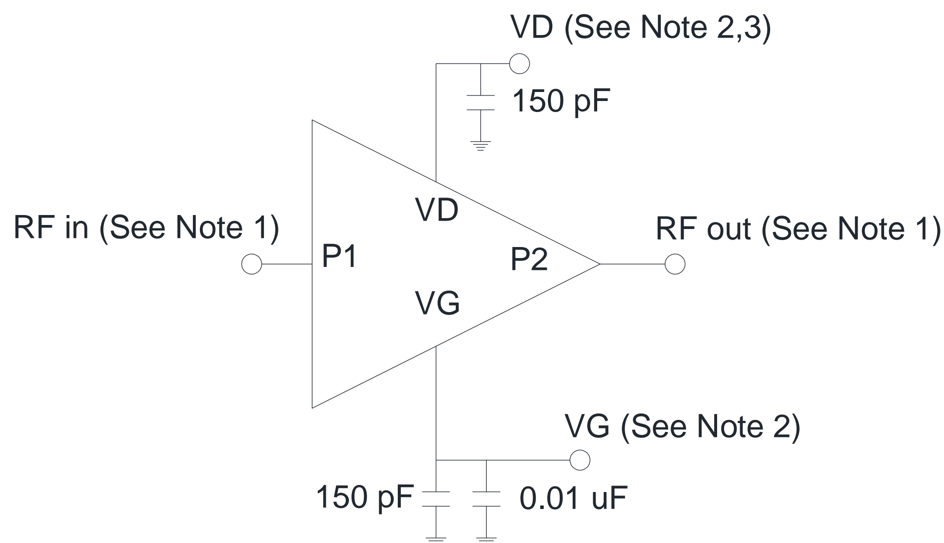
Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
   a) ***Diameter: 25.4 µm (1 mil)***
   b) ***Spacing: 4 mils (~ 100 µm) typical***
   c) ***Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)***
3. ***Wire Length is total length if the wire were made perfectly straight.***

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy only. Eutectic Attach is not recommended though product can be made that supports. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



Note 1: Internal blocking capacitors on RF in/out ports (P1 and P2)
Note 2: Gate Voltage (VG) must be applied prior to Drain Voltage (VD)
Drain Voltage (VD) must be removed prior to Gate Voltage (VG)
Note 3: Performance is optimized with VD set to 8.0V