Wideband Distributed Amplifier, DIE, 1 to 20 GHz

ENGDA00161

Typical Applications

- Military EW and SIGINT
- Receiver or Transmitter
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

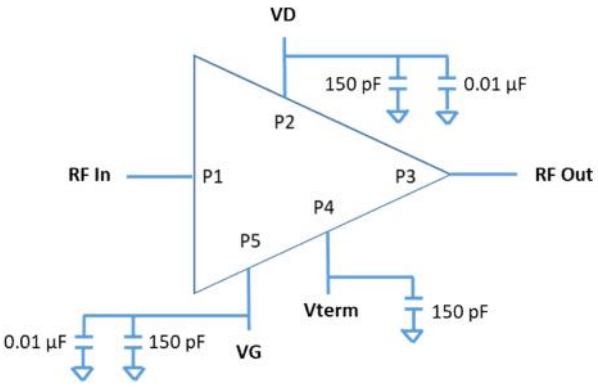
Features

- Wideband performance
- High linearity, 8-dBm IIP3 at 6 V; 10-dBm IIP3 at 8 V
- < 3.0 dB noise figure, 5 – 18 GHz
- 10-dB gain, positive gain slope
- 3 V to 9 V bias operation
- In/out return loss > 16 dB typical
- Size
  - 2.93 x 2.00 x 0.1 mm
  - 0.115 x 0.079 x 0.004 inch

Description

The ENGDA00161 is a wideband, linear GaAs MMIC distributed amplifier die which operates from 1 to 20 GHz. The design is 50 ohm matched and does not require external bias coil inductors. The amplifier delivers 10-dB gain with > 1 dB positive gain slope across the band over a wide drain voltage range (3 V to 9 V). Noise figure is < 3.0 dB across 5 – 18 GHz for bias voltages between 4 and 8 V. The amplifier has gold backside metallization and is designed to be silver epoxy attached. The RF interconnects are designed to account for wire bonds and external microstrip flares for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



ENGIN-IC, Inc.
1721 W. PLANO PKWY STE 121 Plano, TX 75075
Phone 972-332-5000
www.engin-ic.com

Electrical Specifications, T = 25 °C, VD = 6.0 V, 32 mA; 3 V, 4 mA

Parameter	Min	Typ	Max	Units
Frequency Range		1.0 – 20.0		GHz
Gain	8	10	+ slope	dB
Noise Figure		< 3.0 (5-18 GHz)		dB
Input Return Loss	14	18		dB
Output Return Loss	14	19		dB
Output P1dB	7	10		dBm
Output IP3	16	18		dBm
Supply Current	30	30 - 80	100	mA
Thermal Resistance		180		degC/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD	3	6	9	V
ID	30	70	100	mA
VG	-0.2	-0.4	-0.6	V
VTerm	2	3	4	V
Iterm	2	4	6	mA

Absolute Maximum Ratings

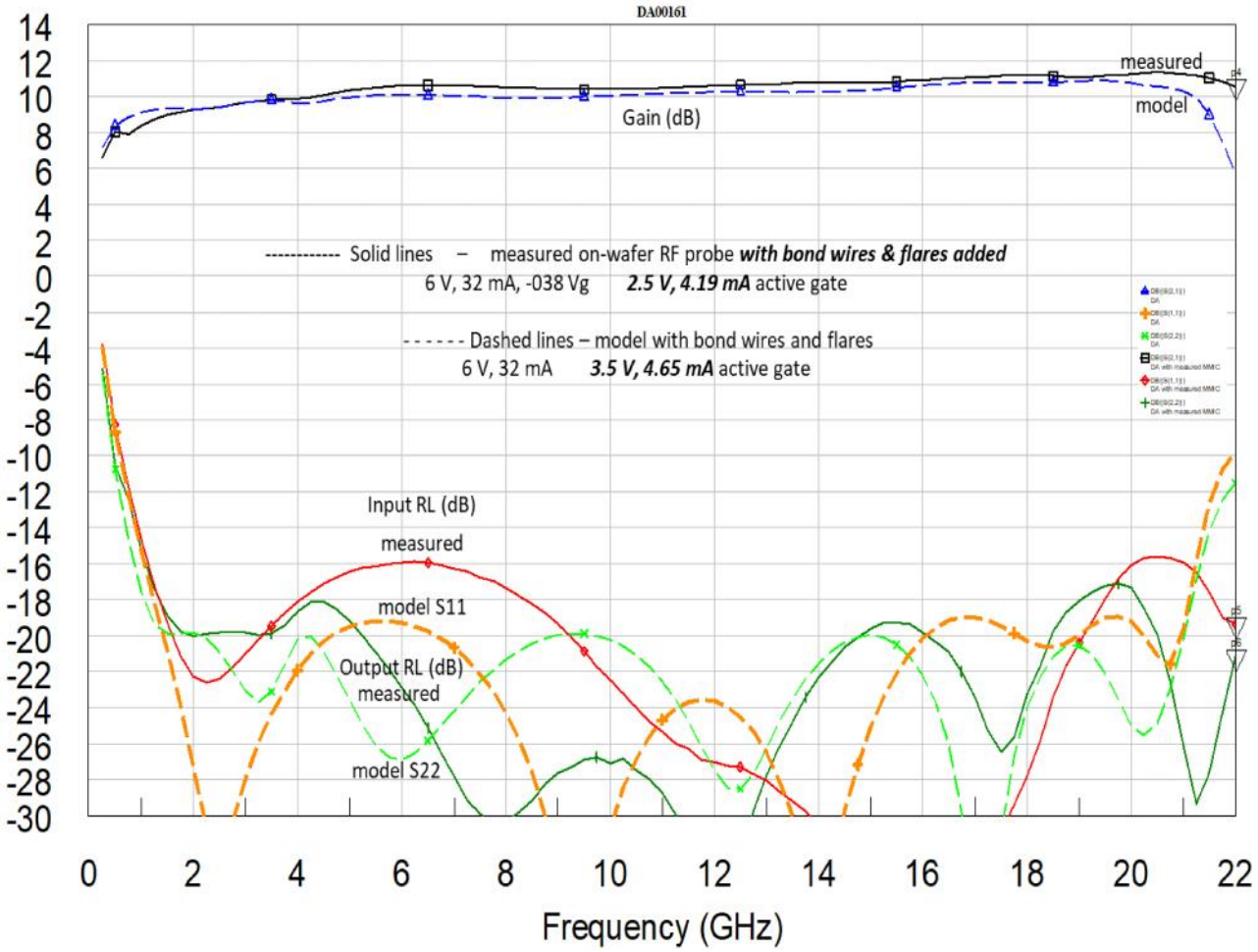
Parameter	Max level
Drain Voltage, VD	10 V
Gate Voltage, VG	-3 V
Active Gate Term., Vterm	5 V
RF Input Power	+24 dBm
Channel temperature	+160 °C
Operating Temperature	-55 °C to +100 °C
Storage Temperature	-65 °C to +150 °C

RF Data with wire bonds and external microstrip flare pads

Gain and Input / Output Return Loss (dB); 6 V, 32 mA, -0.38 Vg
Active gate termination bias: 2.5 - 3 V, 4 mA; 25 °C

Measured – solid lines; model – dashed lines, with bond wires & flares

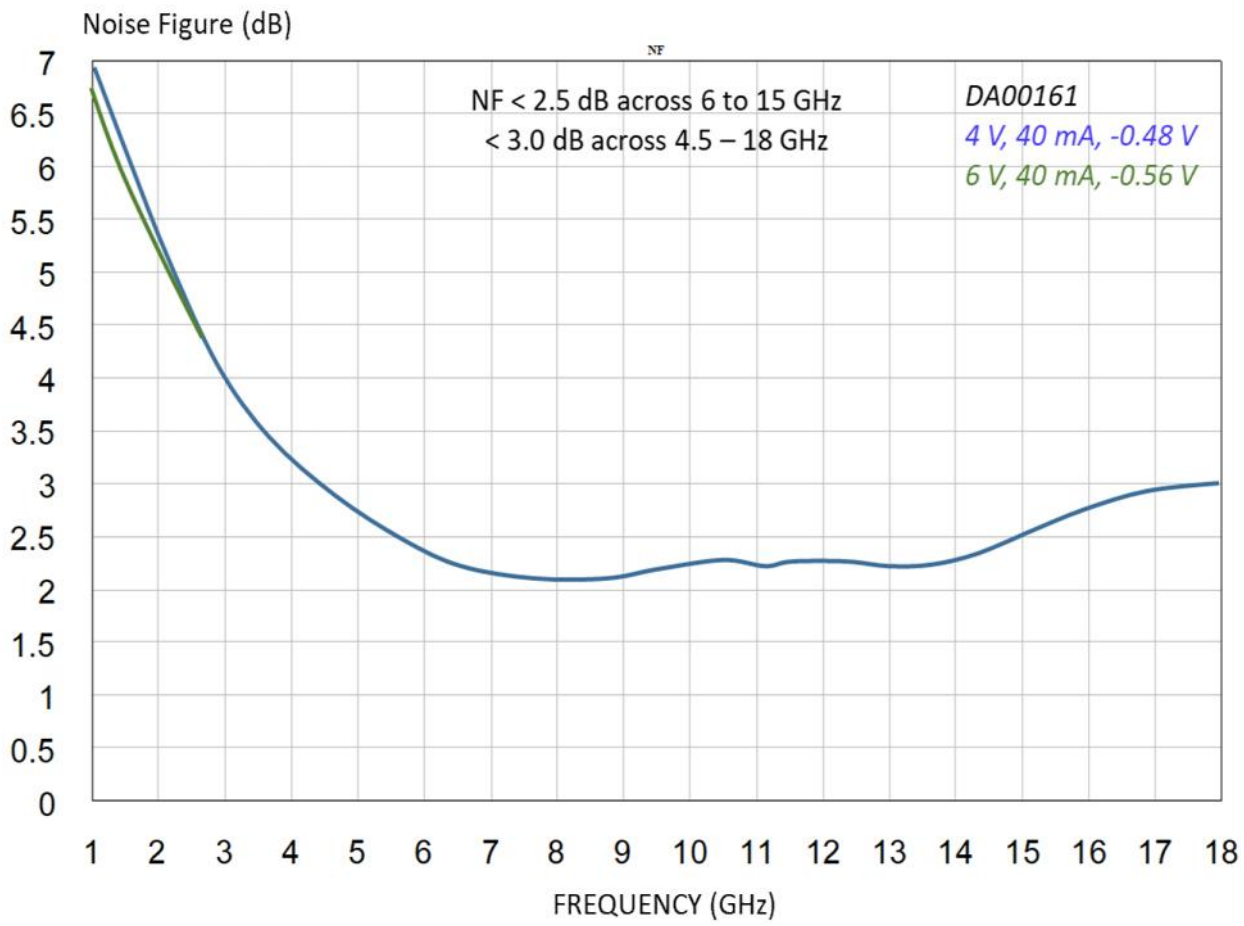
Measured and Modeled Gain are within 0.5 dB across 1 – 20 GHz



RF Data with wire bonds and external microstrip flare pads

Noise figure (dB, at 25 C): VD = 4.0 – 6.0 V, IDS = 40 mA; 25 °C; 3 V, 4 mA

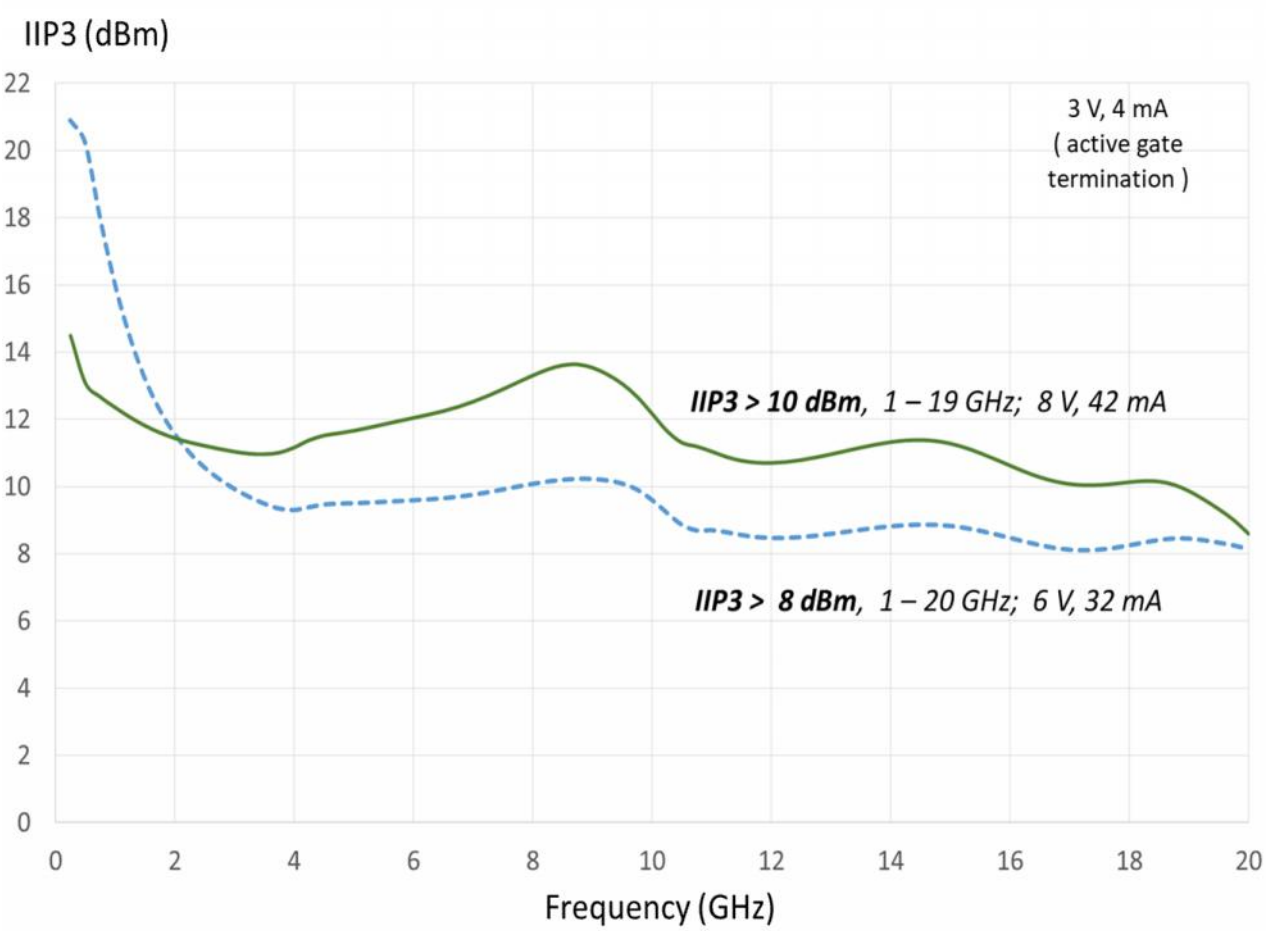
Noise figure varies by only ± 0.1 dB for drain voltages between 4 and 8 V; at 3 V bias, noise figure increases slightly in Ku-band



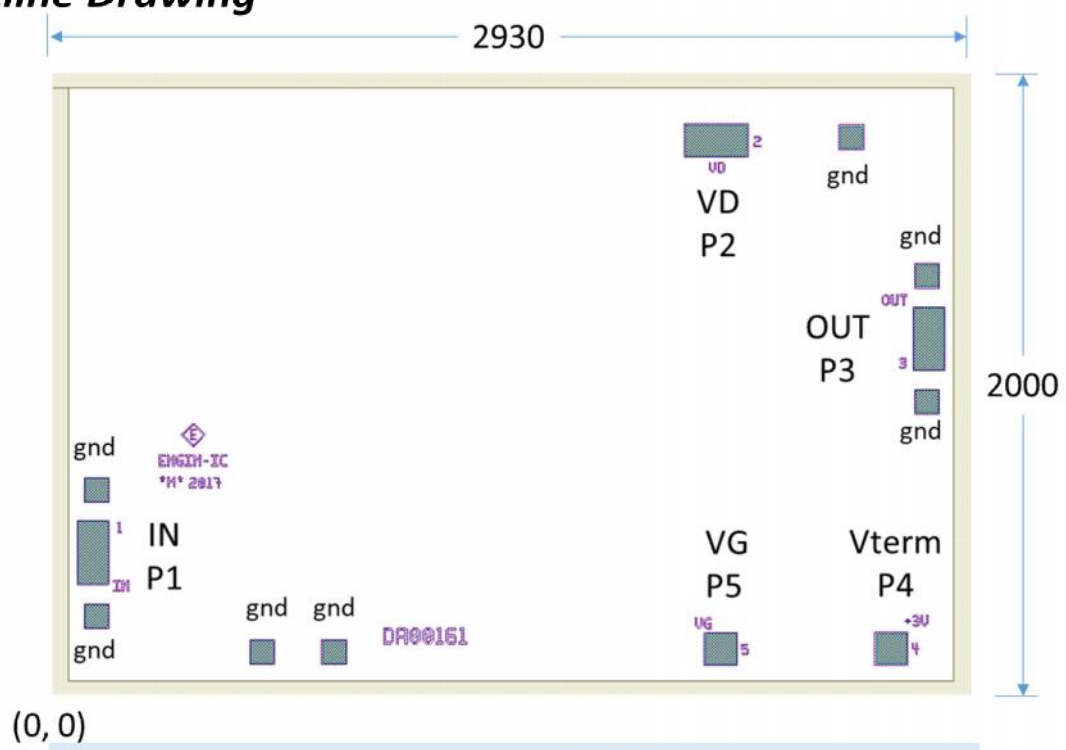
RF Data with wire bonds and external microstrip flare pads

IIP3 > 10 dBm to 19 GHz (OIP3 > 20 dBm);
8 V, 42 mA bias; 3 V, 4 mA active gate term.; 25 °C

IIP3 > 8 dBm to 20 GHz (OIP3 > 18 dBm); 6 V, 32 mA bias



Outline Drawing



	Pad Dimensions			
	Length (x-dim, um)	Width (y-dim, um)	Length (x-dim, mils)	Width (y-dim, mils)
P1 RF Input Pad	100	200	3.94	7.87
P2 VD Drain Bias Pad	200	100	7.87	3.94
P3 RF Output Pad	100	200	3.94	7.87
P4 Vterm Active Term Bias Pad	100	100	3.94	3.94
P5 VG Gate Bias Pad	100	100	3.94	3.94

	Bond Pad Center Point Locations			
	(x-dim, um)	(y-dim, um)	(x-dim, mils)	(y-dim, mils)
P1 RF Input Pad	135	466	5.31	18.35
P2 VD Drain Bias Pad	2115	1774	83.27	69.84
P3 RF Output Pad	2790	1145	109.84	45.08
P4 Vterm Active Term Bias Pad	2670	162	105.12	6.38
P5 VG Gate Bias Pad	2128	162	83.78	6.38

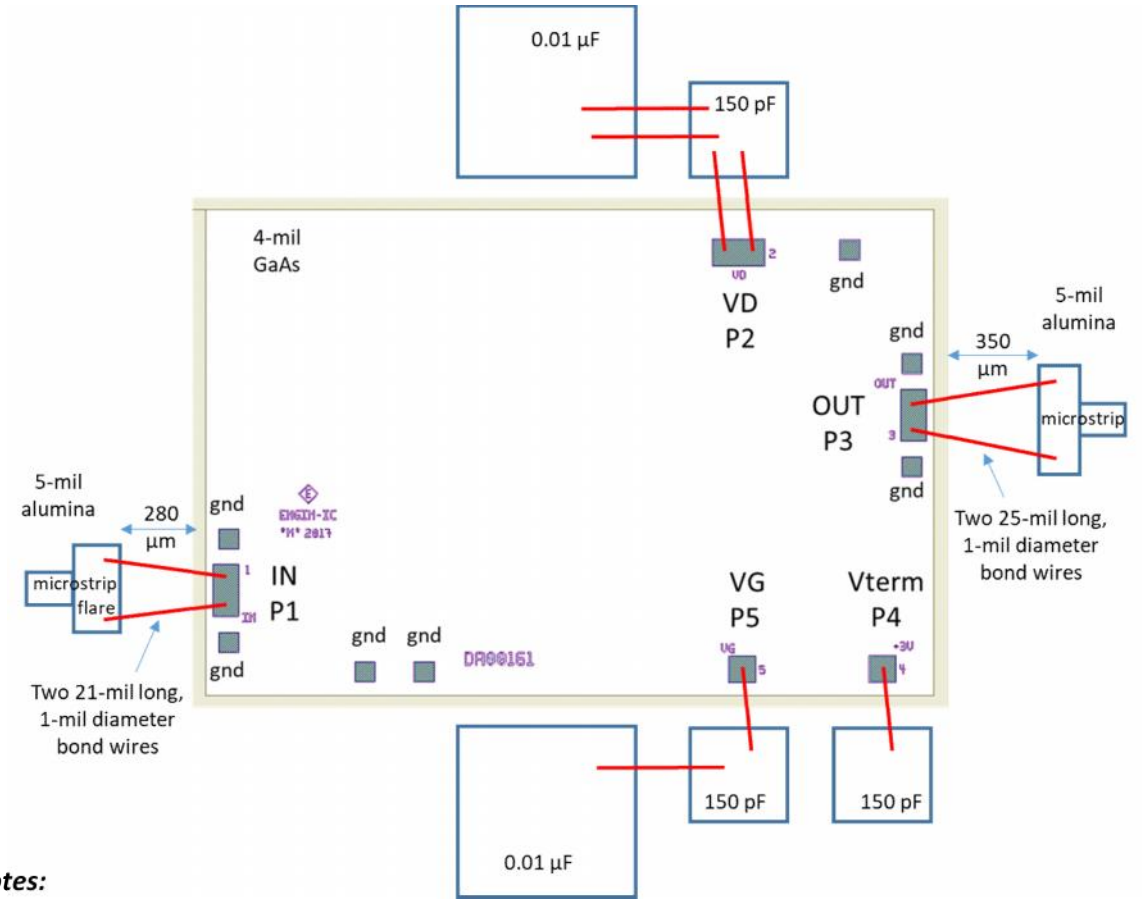
Notes:

1. ***All dimensions are given in both µm and mils. Substrate thickness: 100 µm (0.004").***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

RF I/O Port - External Microstrip Flares on 5-mil Alumina	Length (x-dim, um)	Width (y-dim, um)	Wire Inductance (nH)	Wire Length (um)	# of Wires
P1 RF Input Pad External Flare Dimension	190	346	0.25	533	2
P3 RF Output Pad Ext. Flare Dimension	137	437	0.28	635	2



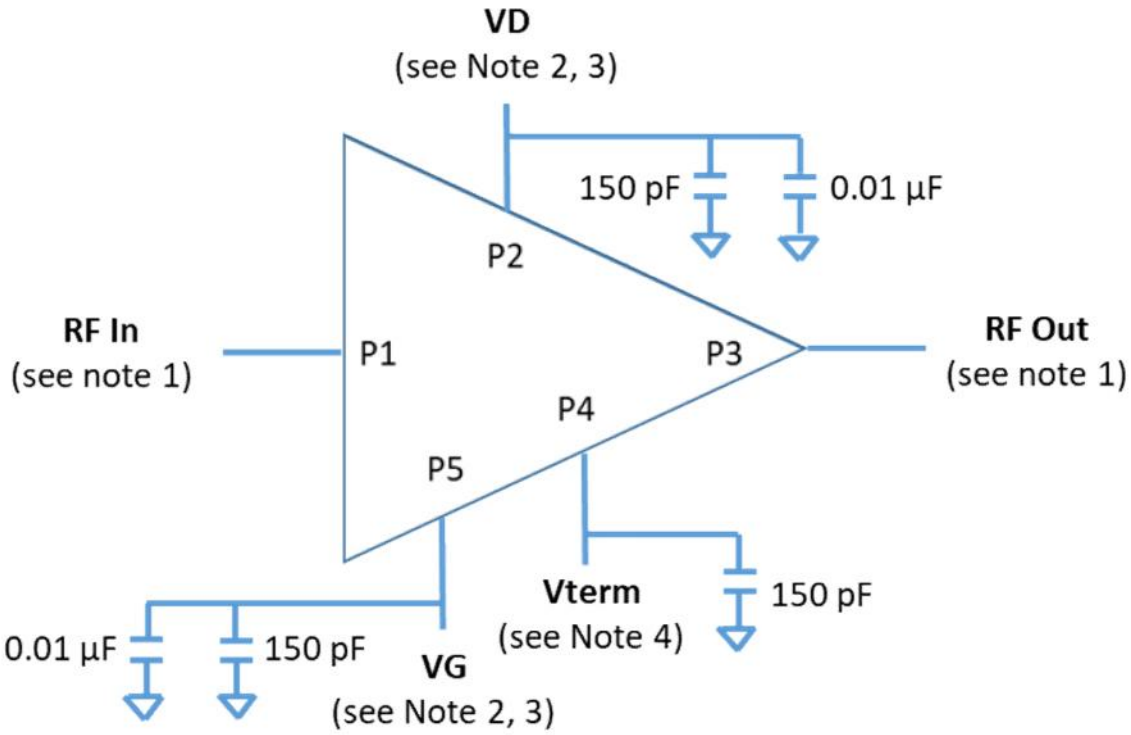
Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
   - ***a) Diameter: 25.4 µm (1 mil)***
   - ***b) Spacing: 127 µm (5 mils) typical***
   - ***c) Height above Ground: 200 µm (~ 8 mils typical); wedge bonds***
3. ***Wire length is total length if the wire were made perfectly straight.***

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy only. This device supports high frequency performance. Care should be made to follow the wire bond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



Note 1: Internal blocking capacitors on RF in/out ports (P1 and P2)
Note 2: Gate voltage (VG) must be applied prior to drain voltage (VD)
Drain voltage (VD) must be removed prior to gate voltage (VG)
Note 3: Performance is optimized with VD set in the 4 to 8 V range
Note 4: Vterm (active gate termination) voltage should normally be near 3 V