Wideband High Gain LNA DIE, 2 to 18 GHz

ENGLA00183A

Typical Applications

- Military and Commercial SATCOM
- Obsolescence Replacement
- Receive or Transmit Circuits
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

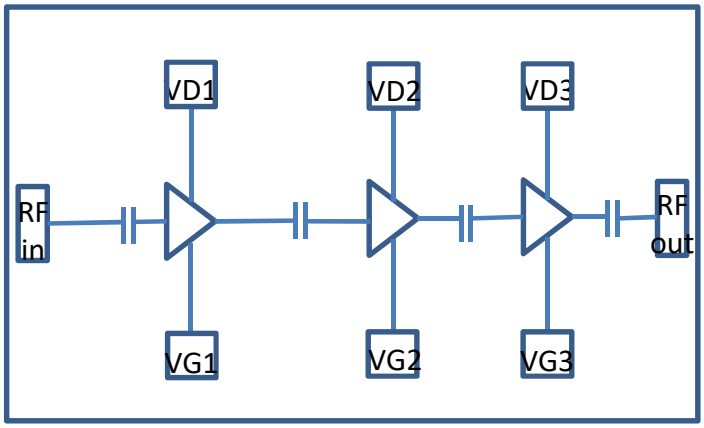
Features

- High Gain 30 – 33 dB
- Low Noise Figure -- 2.7 dB
- Positive Gain Slope
- Good I/O return loss
  - 15 / 12 dB typical
- Size
  - 3.18 x 1.65 x 0.10 mm
  - 0.125 x 0.065 x 0.004 inch

Description

The ENGLA00183A is a Wideband High Gain Low-noise Amplifier (LNA) operating across 2 to 18 GHz. The design is 50 ohm matched and includes on board bias circuitry. The amplifier offers 30-dB gain with 3-dB positive gain slope to overcome high frequency roll–off due to interconnect losses; 2.7-dB de-embedded noise figure; and greater than 25-dBm output third-order intercept point (OIP3) across the band, at room temperature. The MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds to external 50 ohm microstrip lines for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



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Electrical Specifications, T = 25 °C, VD = 3.3 V; ID total = 237 mA

VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA

Parameter	Min	Typ	Max	Units
Frequency Range		2.0 – 18		GHz
Gain	29	32	35	dB
Noise Figure(1)		2.7	3.3	dB
Input Return Loss		15		dB
Output Return Loss		12		dB
Output P1dB		18		dBm
Output IP3	23	27		dBm
Output IP2		TBD		dBm
Supply Current		237		mA
Thermal Resistance(2)		78		°C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD	3.0	3.3	3.6	V
ID		237		mA
VG	-0.25	-0.12	-0.06	V

Absolute Maximum Ratings

Parameter	Max level
Drain Voltage, VD	5.0 V
Gate Voltage, VG	-2.0 V
RF Input Power	+17 dBm
Channel Temperature	+170 °C
Operating Temperature	-55 °C to +100 °C
Storage Temperature	-65 °C to +150 °C

(1) NF De-embedded Input Loss

(2) Channel to MMIC Backside; Backside Temp is 100 °C

Measured Gain and Input/Output Return Loss (dB), with wirebonds and external 50 ohm microstrip line

T = 25 ^{o}C, VD = 3.3 V; ID total = 237 mA

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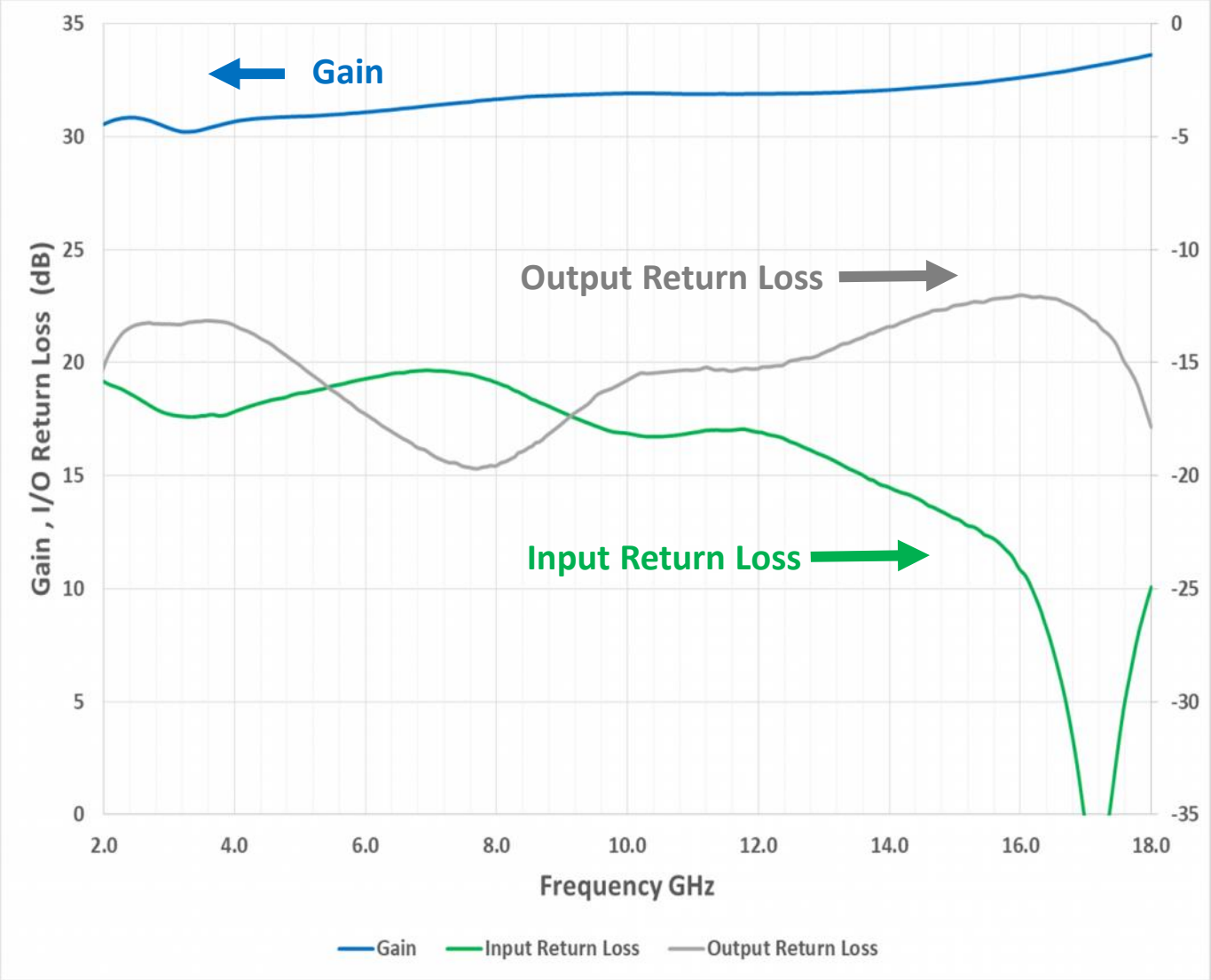
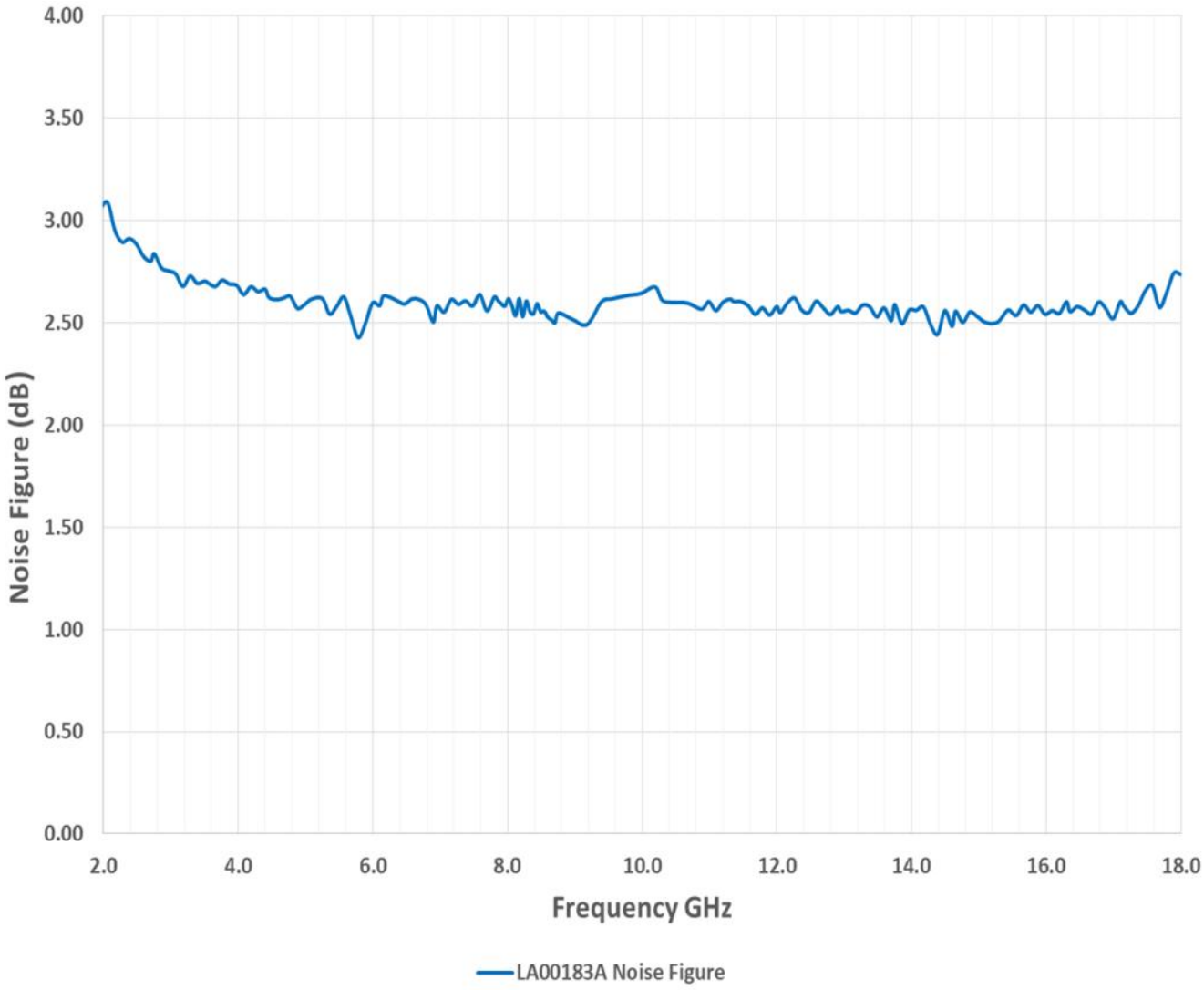


Measured Noise Figure (dB), with wirebonds and external 50 ohm microstrip line

T = 25 ^{o}C, VD = 3.3 V; ID total = 237 mA

VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA

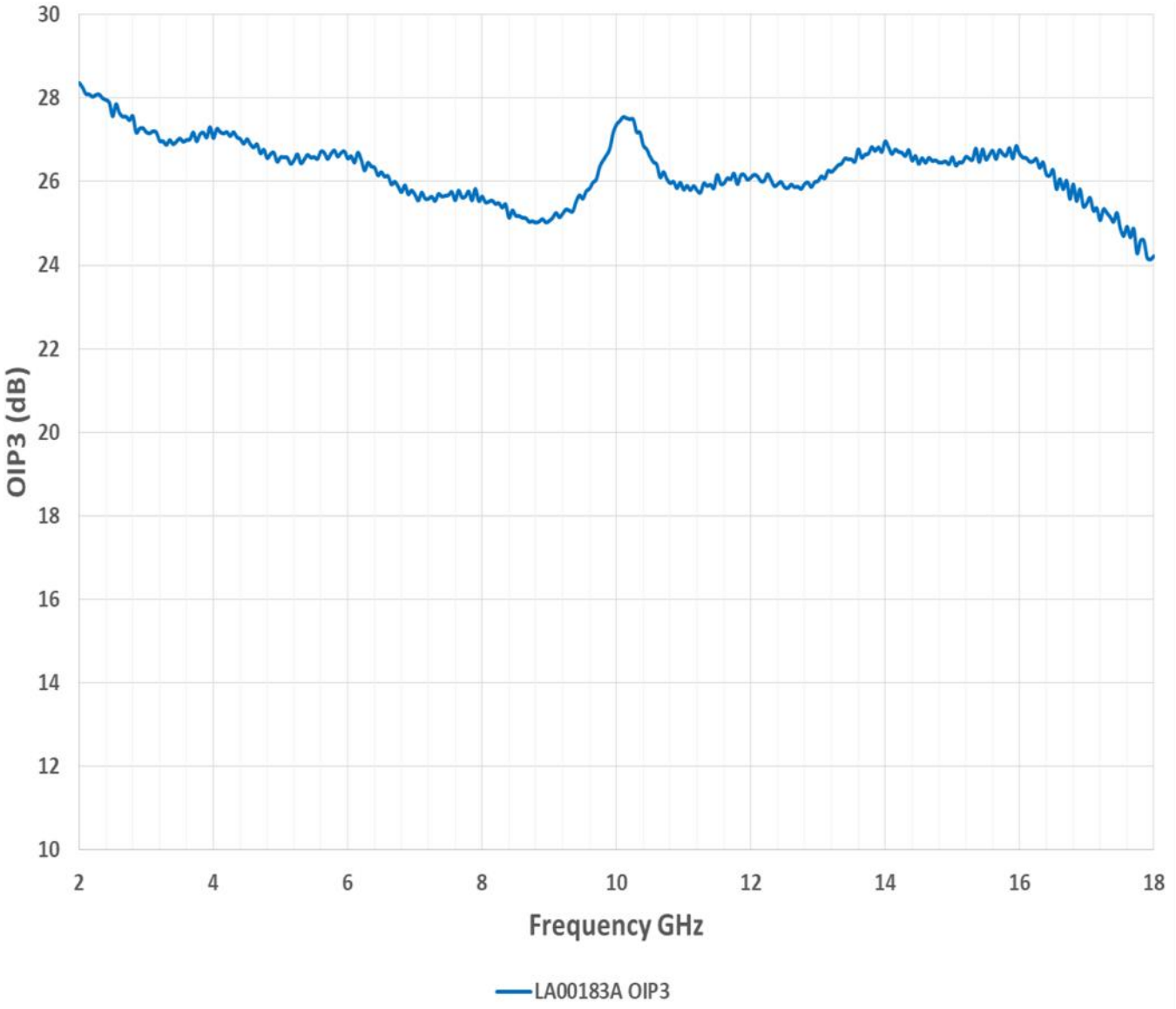


**** Noise Figure De-embedded Input Loss***

Measured Output Third-Order Intercept Point (OIP3, dBm), with wirebonds and external 50 ohm microstrip line

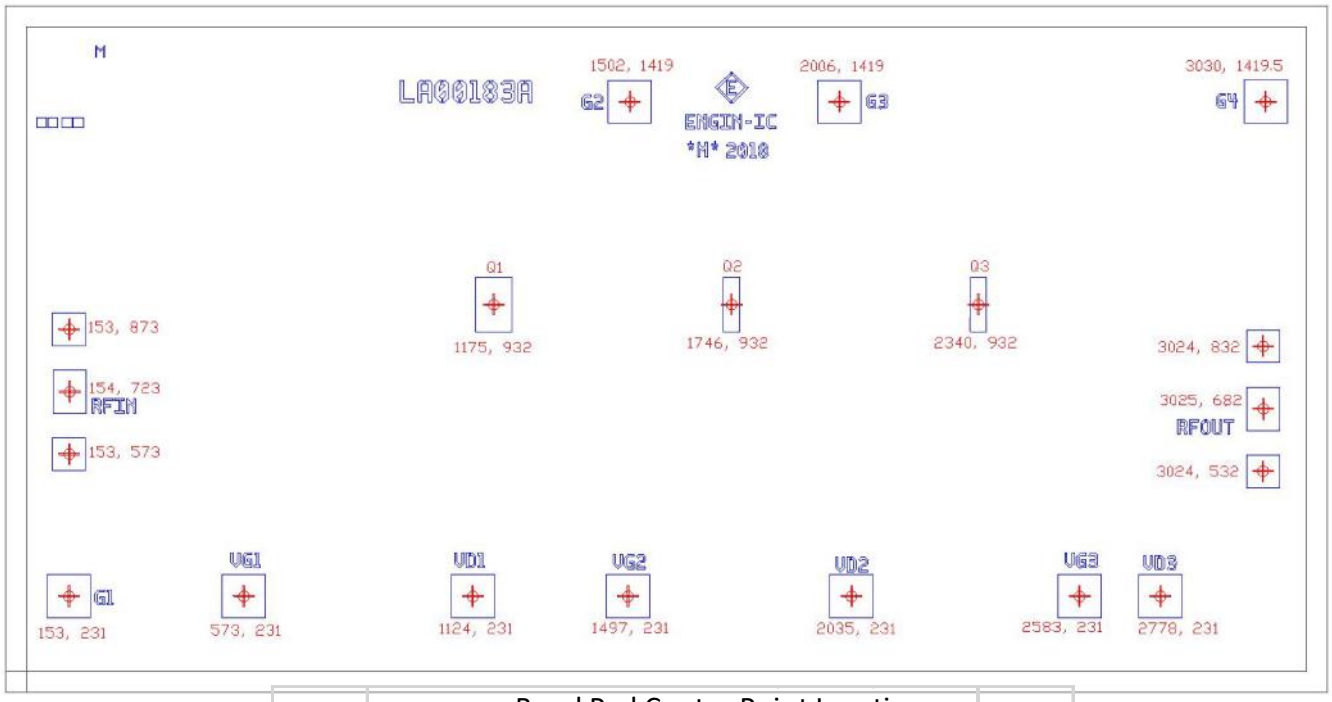
T = 25 ^{o}C, VD = 3.3 V; ID total = 237 mA

VG1 = -0.12 V, ID1 = 114 mA, VG2 = -0.08 V, ID2 = 63 mA, VG3 = -0.08 V, ID3 = 60 mA



MMIC Outline & PAD Location Drawing

3.18mm x 1.65mm



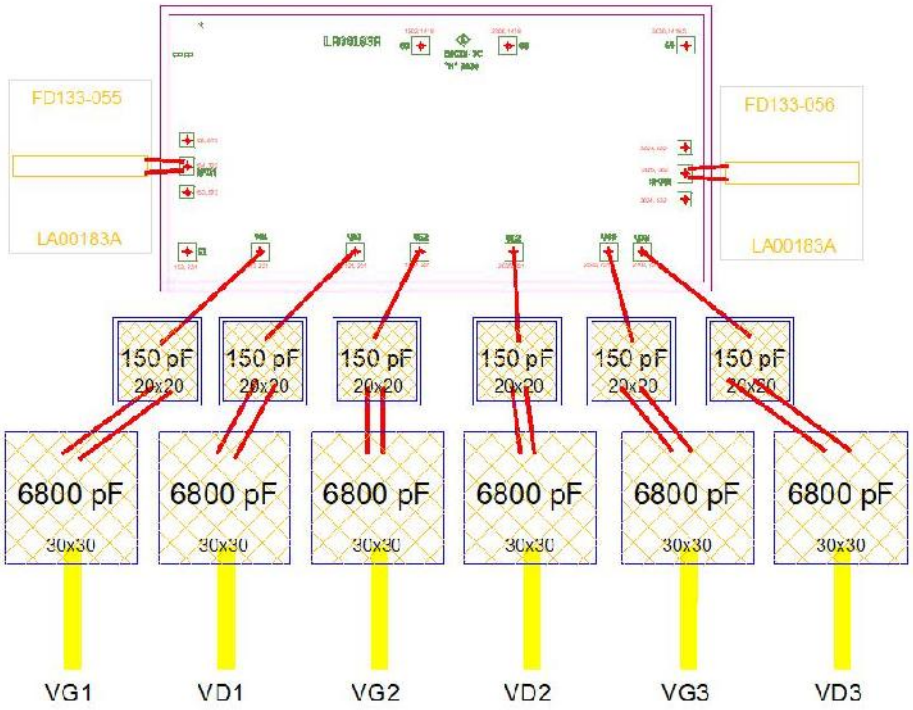
	Bond Pad Center Point Locations				
Pad	Description	Length x-dim (um)	Width y-dim (um)	Length x-dim (mils)	Width y-dim (mils)
RFIN	RF input (port 1)	154	723	6.1	28.5
VG1	VG1 stage 1 gate bias	573	231	22.6	9.1
VD1	VD1 stage 1 drain bias	1124	231	44.3	9.1
VG2	VG2 stage 2 gate bias	1497	231	58.9	9.1
VD2	VD2 stage 2 drain bias	2035	231	80.1	9.1
VG3	VG3 stage 3 gate bias	2583	231	101.7	9.1
VD3	VD3 stage 3 drain bias	2778	231	109.4	9.1
RFOUT	RF output (port 2)	3025	682	119.1	26.9
G1	GND1	153	231	6.0	9.1
G2	GND2	1502	1419	59.1	55.9
G3	GND3	2006	1419	79.0	55.9

Notes:

1. ***Bond pad center locations are given in both µm and mils. Substrate thickness: 100 µm (0.004").***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Line Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level so that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).



	RF I/O - External 50 ohm Microstrip Line on 5-mil Alumina					
	50 ohm	50 ohm	Wire	Wire	Wire	Number
Port	Length	Width	Inductance	Length	Length	of
	x-dim	y-dim				Wires
	(um)	(um)	(nH)	(um)	(mils)	
P1 RF input	775	120	0.115	230	9	2
P2 RF output	775	120	0.115	230	9	2
	50-ohm line					

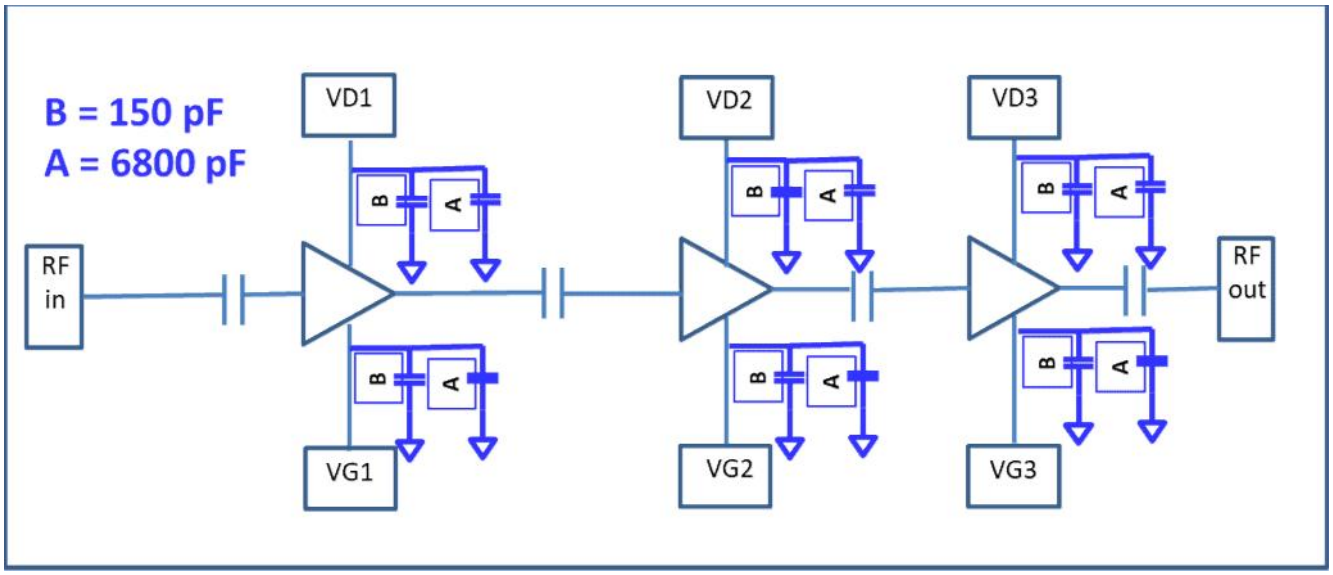
Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external 50 ohm line to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
   - ***a) Diameter: 25.4 µm (1 mil); b) Spacing: 4 mils (~ 100 µm) typical***
   - ***c) Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)***
3. ***Wire Length is total length if the wire were made perfectly straight.***

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports broadband performance . Follow the wirebond dimensions as shown page7 flare diagram for optimum broadband I/O return loss.

Application Circuit and Turn-on Procedure



Note : VD1, VD2, VD3 can be combined after bypass capacitors

Bias Up Sequence :

1. Set Idd limit to 350 mA
2. Set Gate Voltage (VG) = -2.0 V
3. Set Drain Voltage (VD) = 3.3 V
4. Adjust VG1, VG2, VG3 more positive until target ID1,ID2, ID3
5. Turn ON RF Signal

Bias Down Sequence :

1. Turn OFF RF Signal
2. Reduce VG to -2.0 V , Idd should be 0 mA
3. Reduce VD to 0 V
4. Turn OFF DC Supplies