ENGIN·IC

ENGDA00072

Wideband Distributed Amplifier, DIE, 0.8 to 20 GHz

ENGDA00072

Typical Applications

- Military EW and SIGINT
- Receiver or Transmitter
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

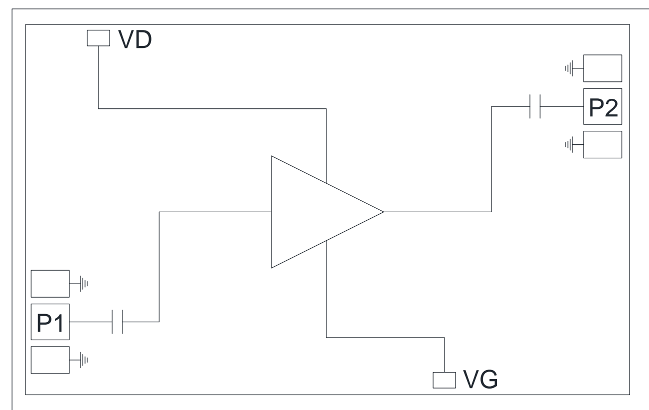
Features

- Wideband Performance
- High Linearity
- 2.5-dB Positive Gain Slope
- Good I/O Return Loss
  - 18 dB typical
- Size
  - 4.0 x 2.48 x 0.1 mm
  - 0.157 x 0.098 x 0.004 inch

Description

The ENGDA00072 is a wideband GaAs MMIC distributed amplifier (DA) die which operates from 0.8 to 20 GHz. The design is 50 ohm matched and includes all required bias circuitry to function to 0.5 GHz. The DA delivers 9 dB gain at 20 GHz with 2.5 dB of positive gain slope across 2 – 20 GHz. The amplifier has gold backside metallization and is designed to be silver epoxy attached. The RF interconnects are designed to account for wire bonds and external microstrip flares for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



Electrical Specifications, T = 25 °C, VD = 9.0 – 10.0 V; VG = -1.0 to -1.2 V

Parameter	Min	Typ	Max	Min	Typ		Units
Frequency Range	0.8 – 10.0			10.0 – 20.0			GHz
Gain	5.5	7		7	8.5		dB
Noise Figure		5.2			5.2		dB
Input Return Loss	15	20		13.5	18		dB
Output Return Loss	15	20		13.5	18		dB
Output P1dB	16	18		16	18		dBm
Output IP3	32	34		30	32		dBm
Output IP2	38	40		40	43		dBm
Supply Current	110	130	150	110	130	150	mA
Thermal Resistance		80			80		degC/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD	9	9 - 10	10	V
ID		110		mA
VG	-1.0	-1.1	-1.2	V

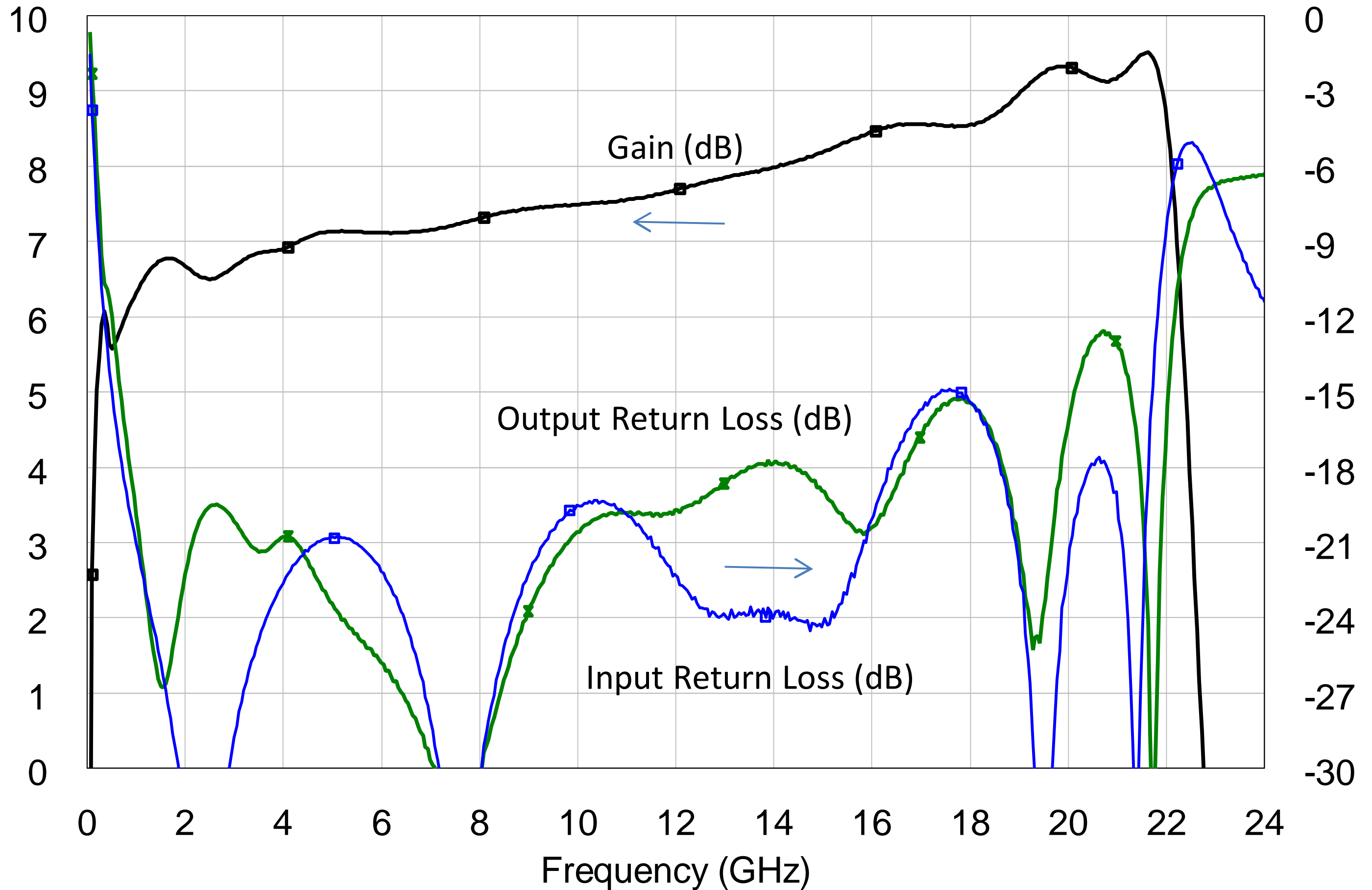
Absolute Maximum Ratings

Parameter	Max level
Drain Voltage, VD	12 V
Gate Voltage, VG	-6 V
RF Input Power	+27 dBm
Channel temperature	+165 °C
Operating Temperature	-55 °C to +100 °C
Storage Temperature	-65 °C to +150 °C

ENGIN-IC, Inc
1721 W. PLANO PKWY STE 121 Plano, TX 75075
Phone 972-332-5000
www.engin-ic.com

Measured RF Data with wirebonds and external microstrip flares

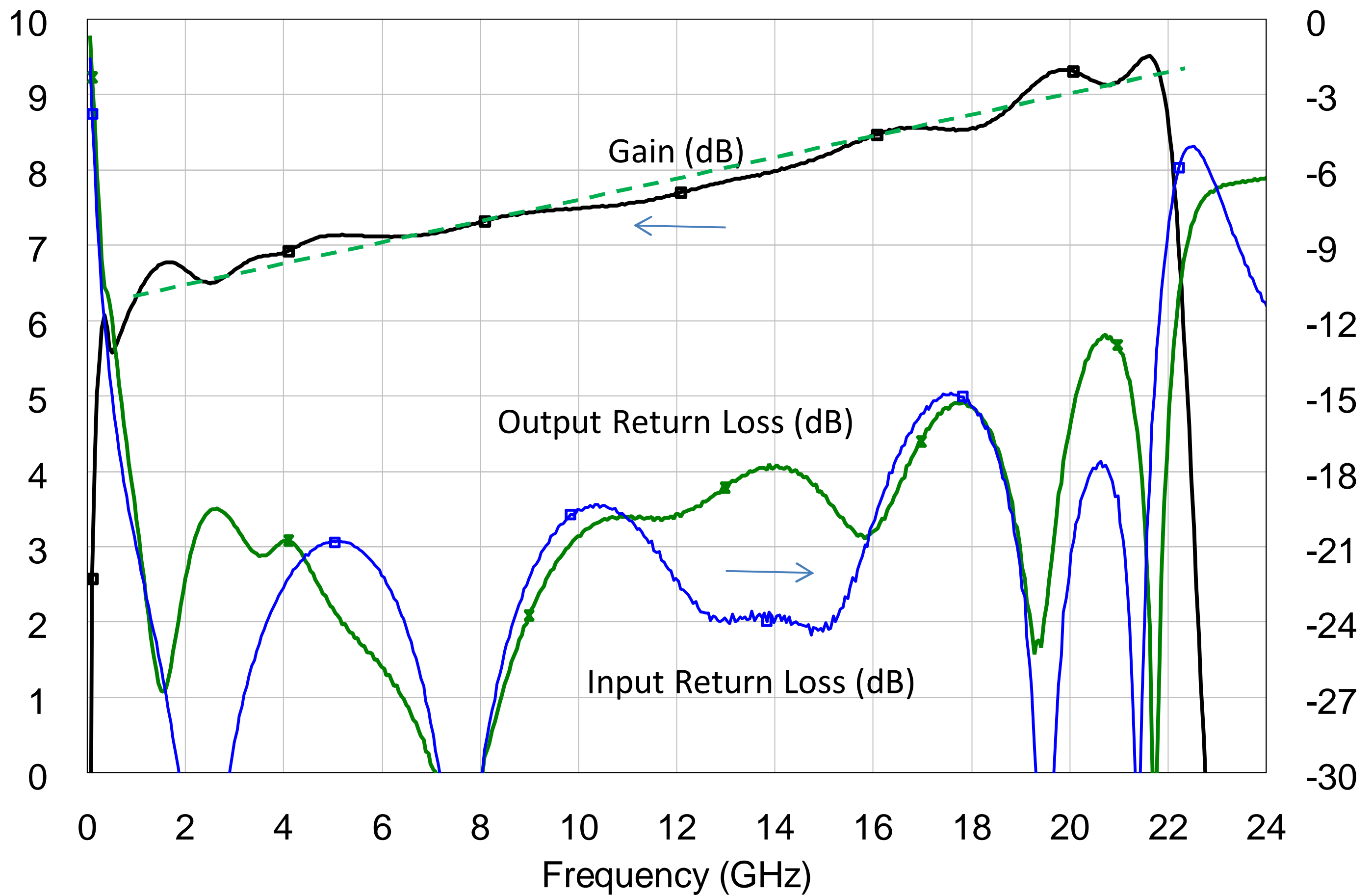
Gain and Input / Output Return Loss (dB); 10 V, 114 mA, -1.4 Vg



Measured RF Data with wirebonds and external microstrip flares

Gain and Input / Output Return Loss (dB); 10 V, 114 mA, -1.4 Vg

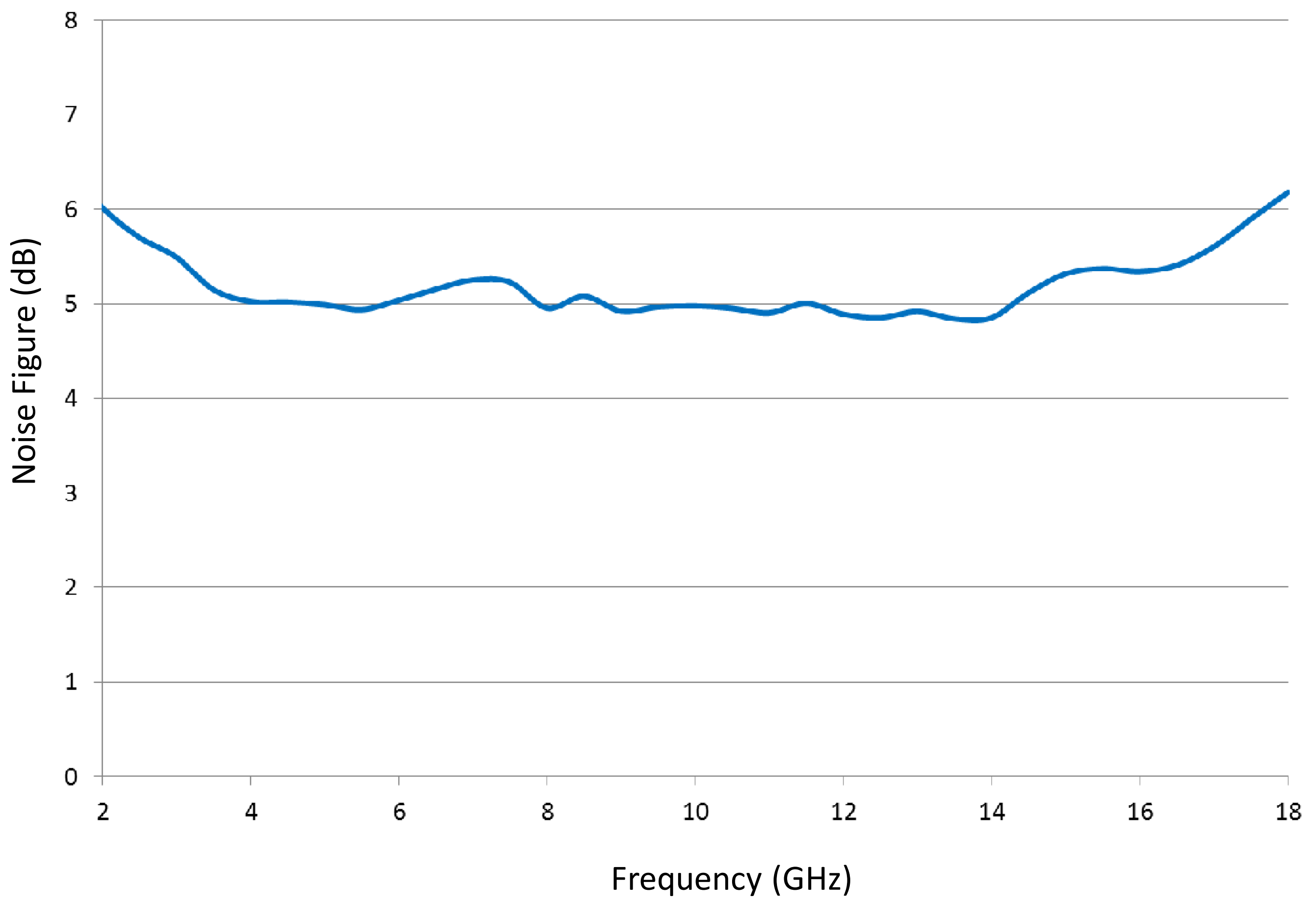
Positive Gain Slope = 2.5 dB from 2 to 20 GHz



RF Data with wirebonds and external microstrip flare pads

Measured Noise Figure (dB)

VD = 10.0 V, VG = -1.0 V, ID = 146 mA; room temperature

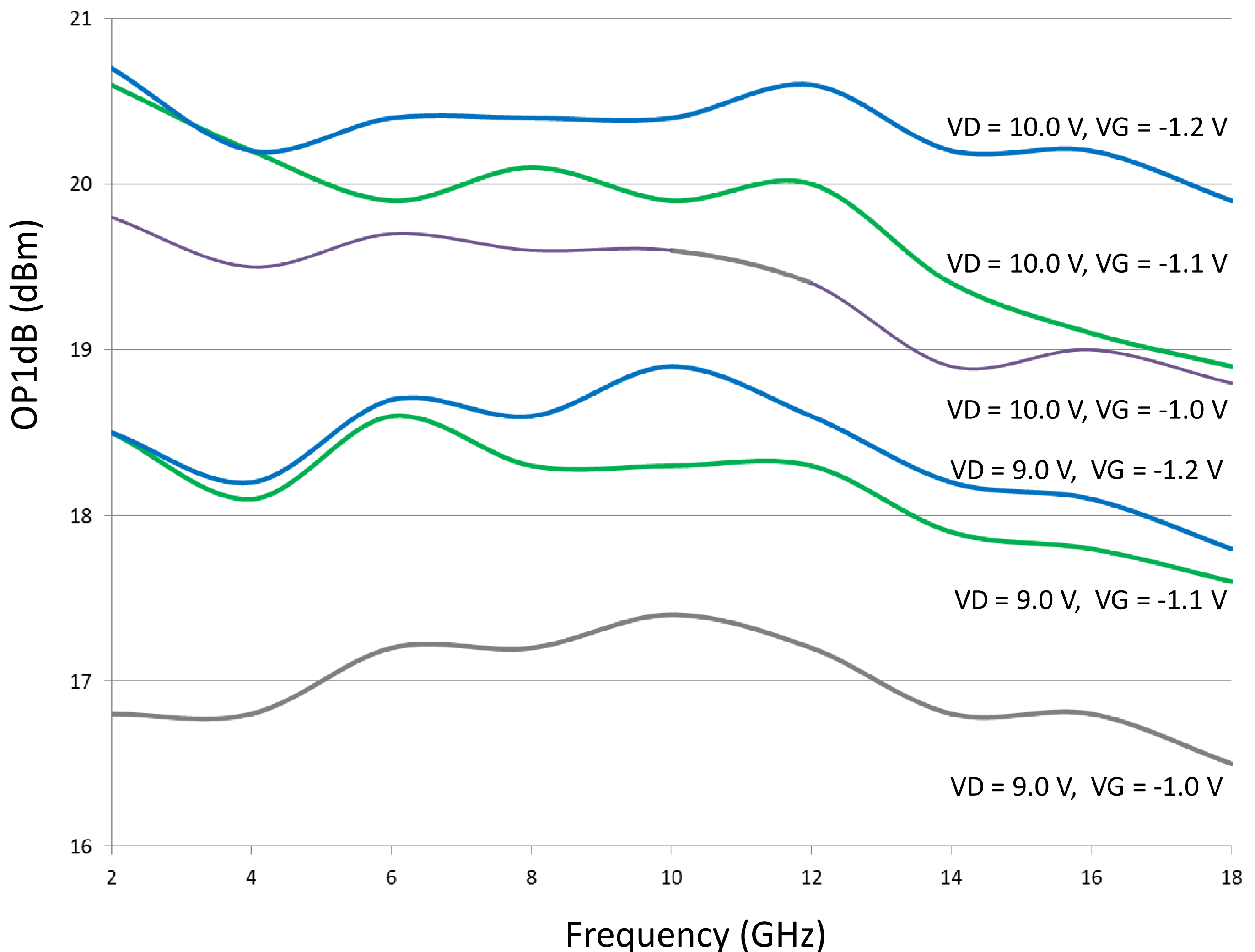


RF Data with wirebonds and external microstrip flare pads

Measured Output Power at 1-dB Gain Compression (OP1dB, dBm)

VD = 9 and 10 V; VG = -1.0, -1.1, and -1.2 V; room temperature

OP1dB = 20 dBm (10 V, -1.2 Vg); 18 dBm (9 V, -1.2 Vg)



RF Data with wirebonds and external microstrip flare pads

Measured Output Power at 1-dB Gain Compression (OP1dB, dBm)

VD = 9 and 10 V; VG = -1.0, -1.1, and -1.2 V; room temperature

DA00072 1-dB gain compression

VD	V	9	9	9	10	10	10
Iquiescent	mA	142	134	123	146	136	126
VG	V	-1	-1.1	-1.2	-1	-1.1	-1.2
	Freq (GHz)			OP1dB (dBm)			
	2	16.8	18.5	18.5	19.8	20.6	20.7
	4	16.8	18.1	18.2	19.5	20.2	20.2
	6	17.2	18.6	18.7	19.7	19.9	20.4
	8	17.2	18.3	18.6	19.6	20.1	20.4
	10	17.4	18.3	18.9	19.6	19.9	20.4
	12	17.2	18.3	18.6	19.4	20.0	20.6
	14	16.8	17.9	18.2	18.9	19.4	20.2
	16	16.8	17.8	18.1	19.0	19.1	20.2
	18	16.5	17.6	17.8	18.8	18.9	19.9

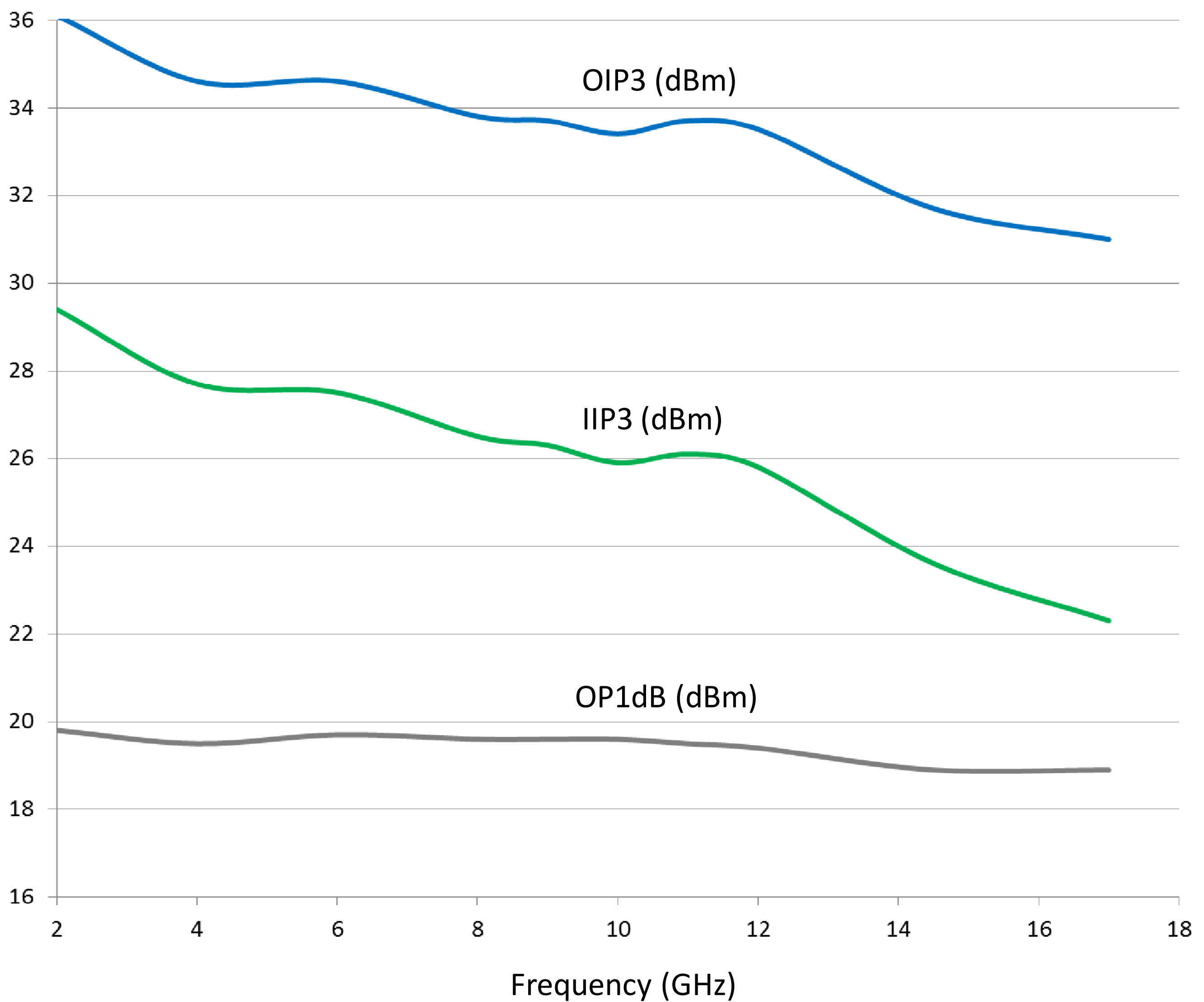
RF Data with wirebonds and external microstrip flare pads

MEASURED IIP3 and OIP3 (dBm); 10 V, 146 mA, -1.0 Vg;

0 dBm per tone; 2 MHz spacings

OIP3 > 31 dBm to 17 GHz; IIP3 > 22 dBm

OP1dB > 18.5 dBm to 18 GHz; OIP3 / OP1dB varies from 12.1 to 16.3 dB



ENGIN-IC, Inc
1721 W. PLANO PKWY STE 121 Plano, TX 75075
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RF Data with wirebonds and external microstrip flare pads

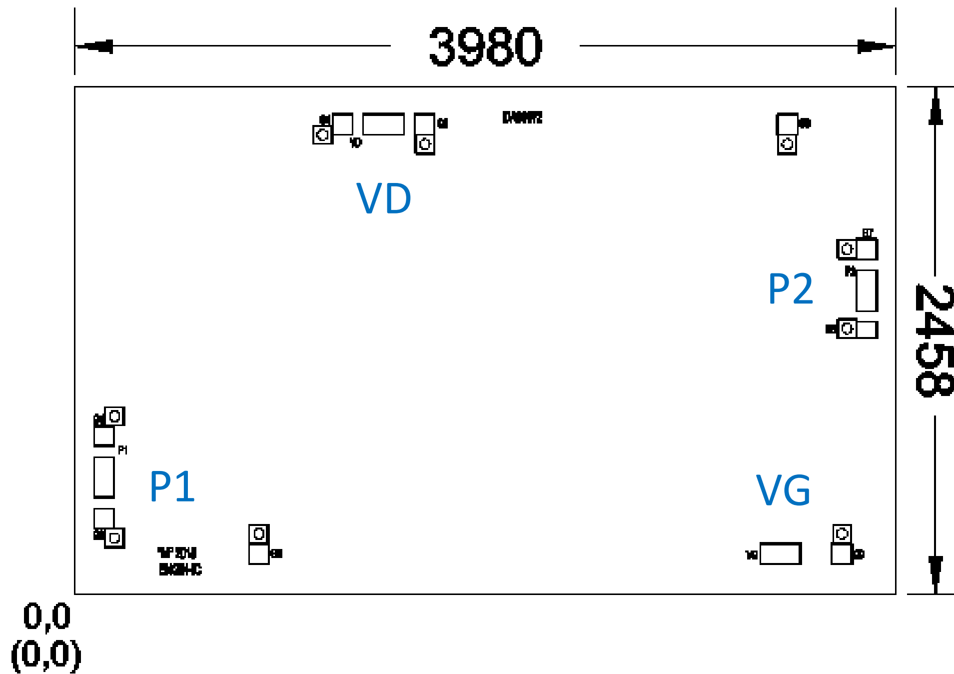
Measured OIP2(dBm); 10 V, 146 mA, -1.0 Vg;

OIP2 > 40 dBm, 3 – 18 GHz

0 dBm per tone

F1 (GHz)	F2 (GHz)	IIP2 (dBm)	OIP2 (dBm)
2	2.002	32.5	39.3
5	5.002	33.0	40.1
8	8.002	33.5	40.8
9	9.002	33.5	40.9
10	10.002	32.5	40.0
12	12.002	34.0	41.7
8	10	36.0	43.4
10	12	37.3	44.9
12	14	35.8	43.6
14	16	33.7	41.9
16	18	34.0	42.6

Outline Drawing



	Pad Dimensions			
	Length (x-dim, um)	Width (y-dim, um)	Length (x-dim, mils)	Width (y-dim, mils)
P1 RF Input Pad Dimension	100	200	3.937	7.874
P2 RF Output Pad Dimensions	100	200	3.937	7.874
VD Drain Bias Pad Dimension	200	100	7.874	3.937
VG Gate Bias Pad Dimension	200	100	7.874	3.937

	RF Bond Pad Center Point Locations			
	x-dim, um	y-dim, um	x-dim, mils	y-dim, mils
P1 RF Input Pad Location	140	567.5	5.512	22.343
P2 RF Output Pad Location	3840	1473	151.181	57.99
VD Drain Bias Pad Location	1495.5	2278.2	58.878	89.693
VG Gate Bias Pad Location	3420	196	134.646	7.717

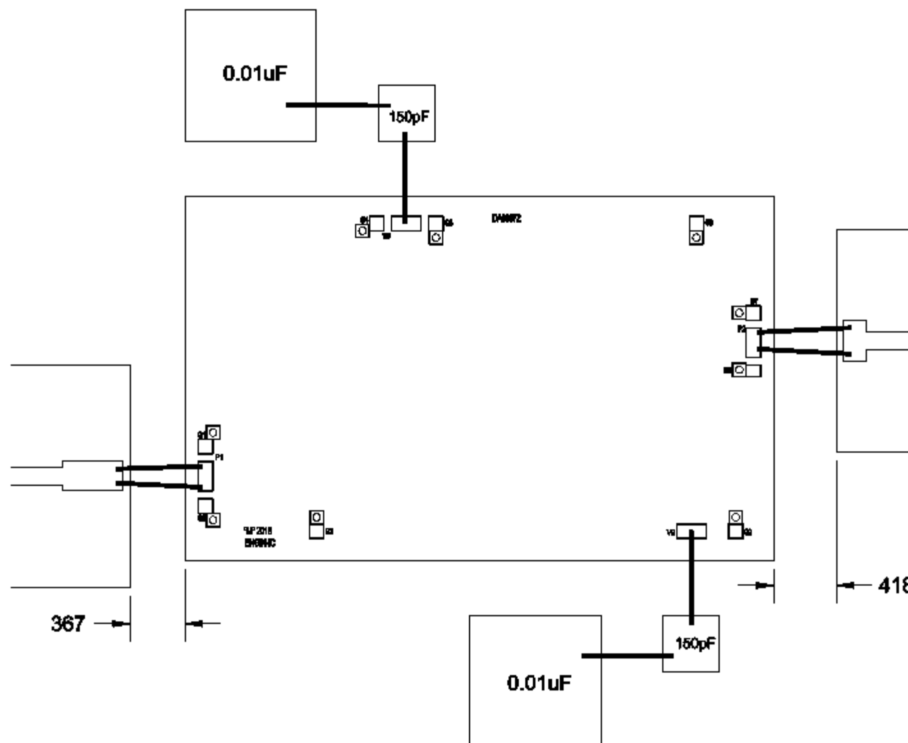
Notes:

1. ***All dimensions are given in both µm and mils. Substrate thickness: 100 µm (0.004”).***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

	RF I/O port - External Microstrip Flares on 5-mil Alumina				
	Flare Width y-dim, um	Flare Length x-dim, um	Wire Inductance (nH)	Wire Length (um)	Number of Wires
P1 RF Input Pad Flare Dimension	195	408	0.265	583	2
P2 RF Output Pad Flare Dimension	277	157	0.295	630	2



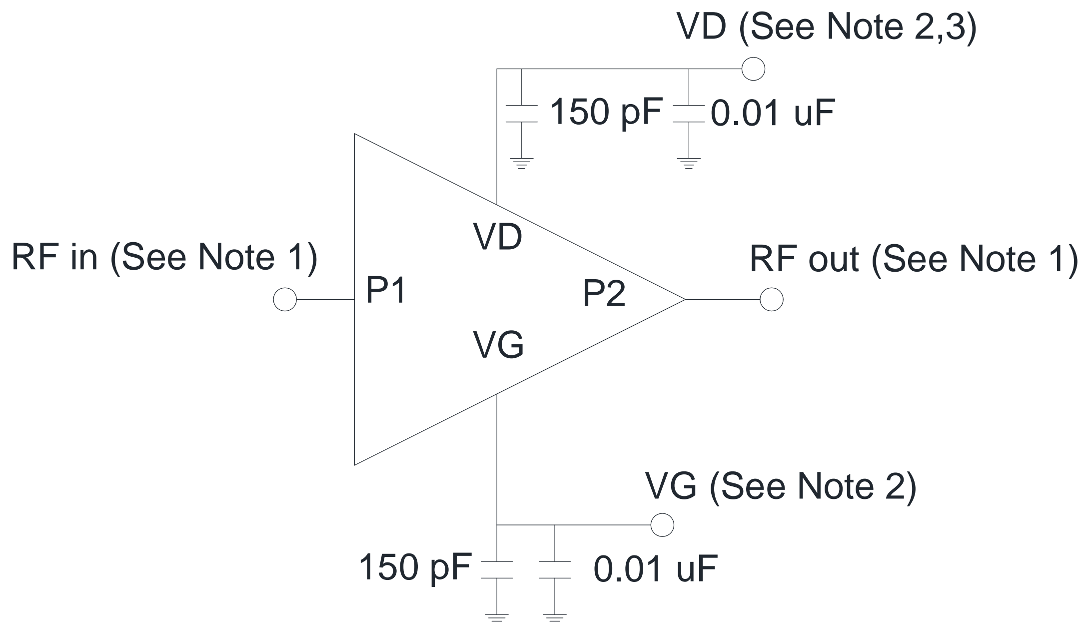
Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
    a) ***Diameter: 25.4 µm (1 mil)***
    b) ***Spacing: 4 mils (~ 100 µm) typical***
    c) ***Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)***
3. ***Wire Length is total length if the wire were made perfectly straight.***

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy only. Eutectic Attach is not recommended though product can be made that supports. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



Note 1: Internal blocking capacitors on RF in/out ports (P1 and P2)
Note 2: Gate Voltage (VG) must be applied prior to Drain Voltage (VD)
Drain Voltage (VD) must be removed prior to Gate Voltage (VG)
Note 3: Performance is optimized with VD set to 8.0V