ENGIN·IC

ENGLA00096C

Wideband LNA, DIE, 18 to 50 GHz

ENGLA00096C

Typical Applications

- Military and Commercial SATCOM
- Obsolescence Replacement
- Receive or Transmit Circuits
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

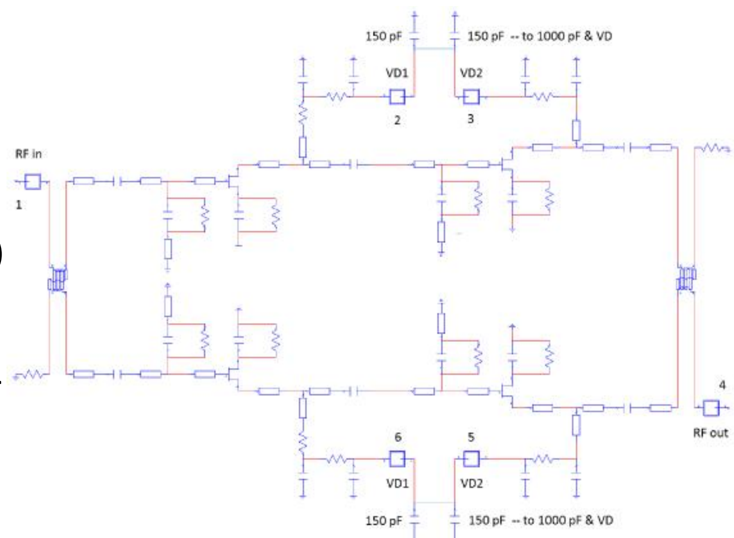
Features

- 18 to 50 GHz band coverage
- Low Noise Figure (2.3 dB typical)
- 11-dB Gain at 2 - 3 V, 80 mA bias
- Good I/O return loss (14 dB typ.)
- Self-biased (single supply voltage)
- Size
    - 2.80 x 1.80 x 0.10 mm
    - 0.110 x 0.071 x 0.004 inch

Description

The ENGLA00096C is a wideband low-noise amplifier (LNA) operating across 18 to 50 GHz. The design is 50 ohm matched and includes on board bias circuitry. The amplifier offers 11-dB gain, 2.3 dB noise figure, and 23-dBm output third-order intercept point (OIP3) above 40 GHz, at room temperature. The GaAs MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds and external microstrip flares for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



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Electrical Specifications, T = 25 °C, VD = 3.0 V

Parameter	Min	Typ	Max	Units
Frequency Range	18.0 – 50.0			GHz
Gain	9.5	11.5		dB
Noise Figure		2.3 (20 – 50 GHz)	3.3 (20 – 50 GHz)	dB
Input Return Loss	11	15		dB
Output Return Loss	11	14		dB
Output P1dB		-7 (18 GHz) to +12 (51 GHz) (-4 to +16 dBm at 4 V bias)		dBm
Output IP3		+6 (18 GHz) to +25 (51 GHz) (+9 to +25 dBm at 4 V bias)		dBm
Output IP2		+14 (18 GHz) to +45 (51 GHz) (+17 to +45 dBm at 4 V bias)		dBm
Supply Current	55	60 - 120	140	mA
Thermal Resistance *		115 * includes 25-µm thick AuSn solder mount		°C/W

Recommended Operating Conditions

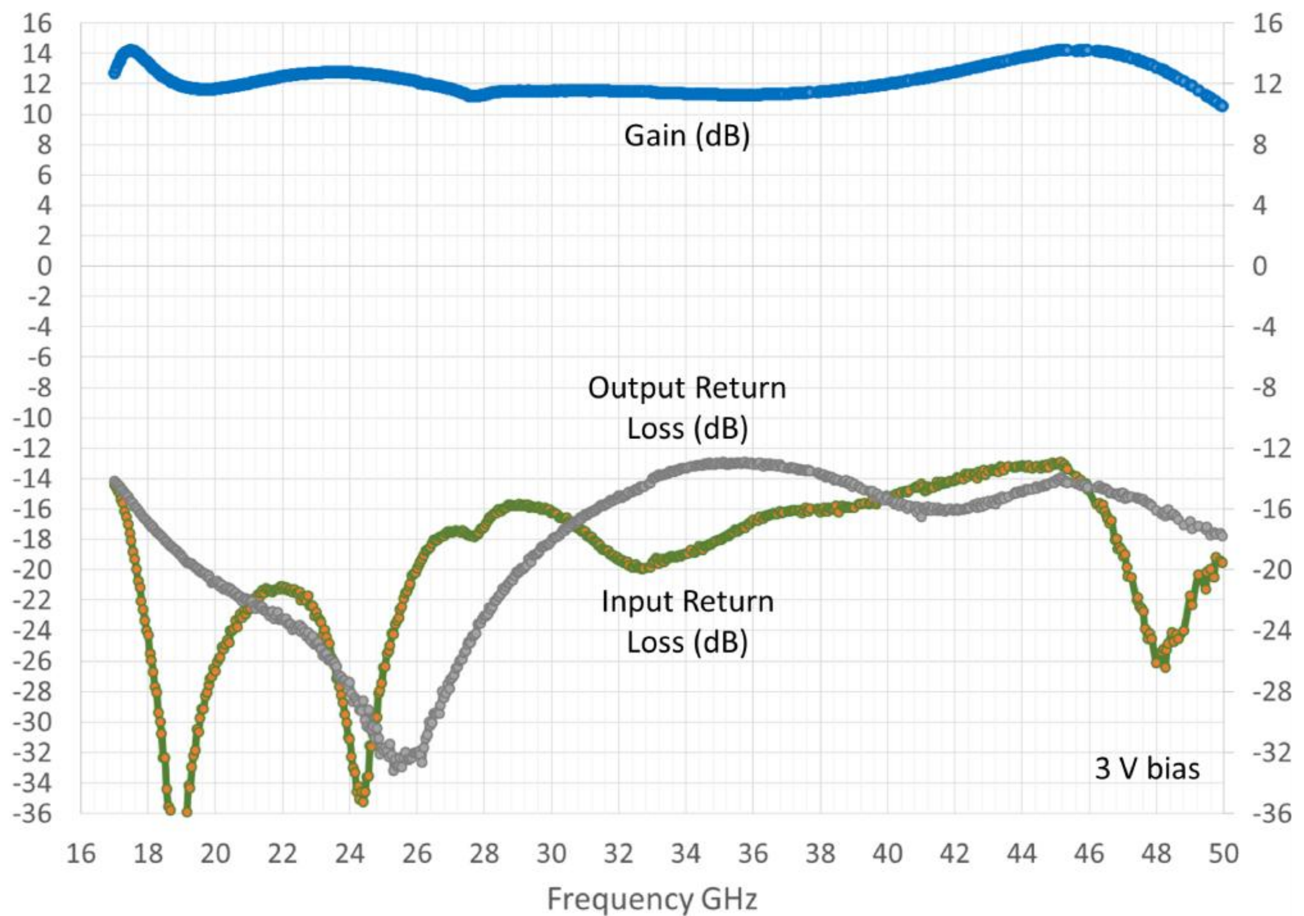
Parameter	Min	Typ	Max	Units
VD	1.5	2 - 4	4.5	V
ID	55	60 - 120	140	mA
VG		self-bias		V

Absolute Maximum Ratings

Parameter	Max level
Drain Voltage, VD	5.5 V
Gate Voltage, VG	N/A; self-biased
RF Input Power	+17 dBm
Channel Temperature	+165 °C
Operating Temperature	-55 °C to +100 °C
Storage Temperature	-65 °C to +150 °C

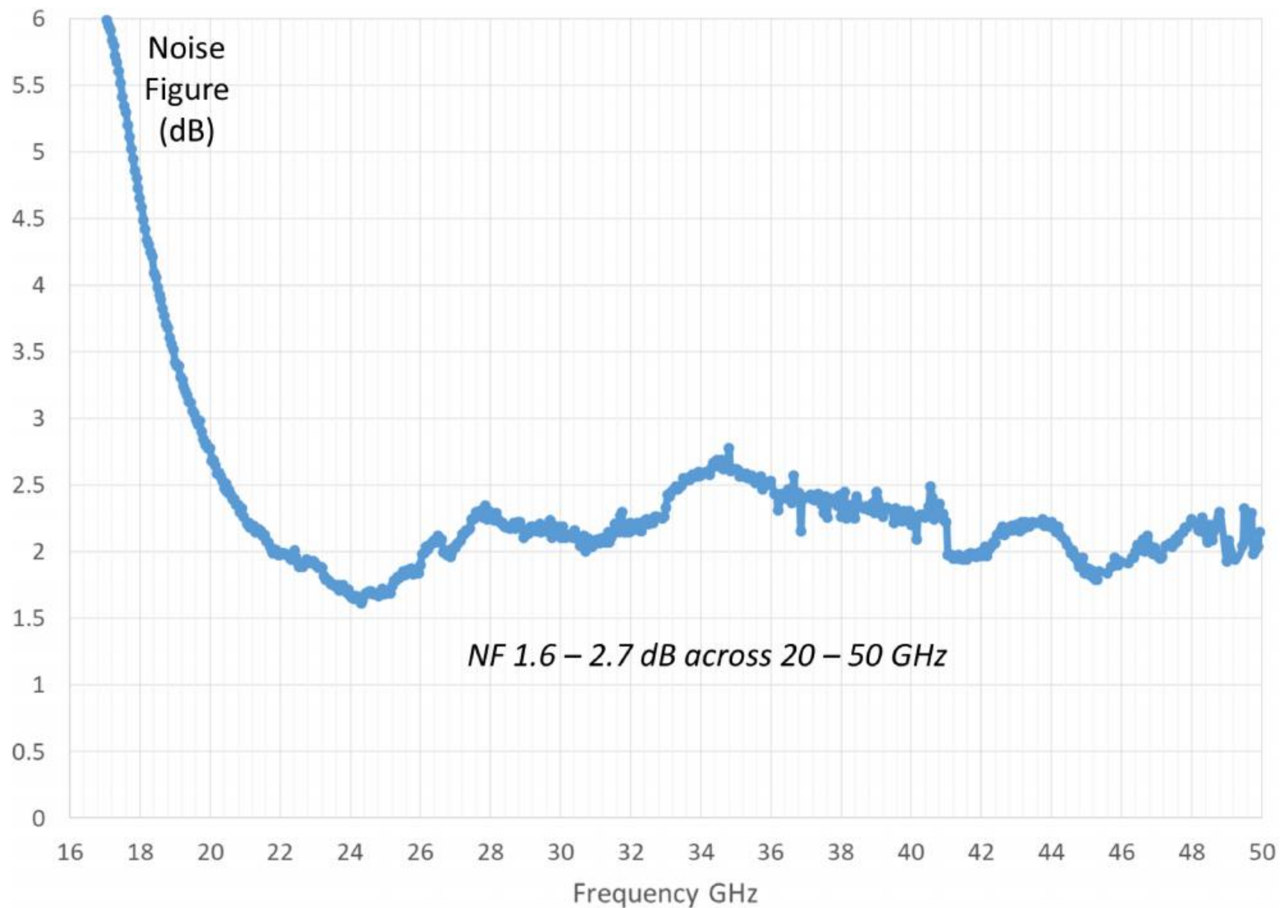
Measured Gain and Input/Output Return Loss (dB), with wirebonds to external 50-ohm microstrip lines

VD = 3.0 V; ID = 72 mA; room temperature



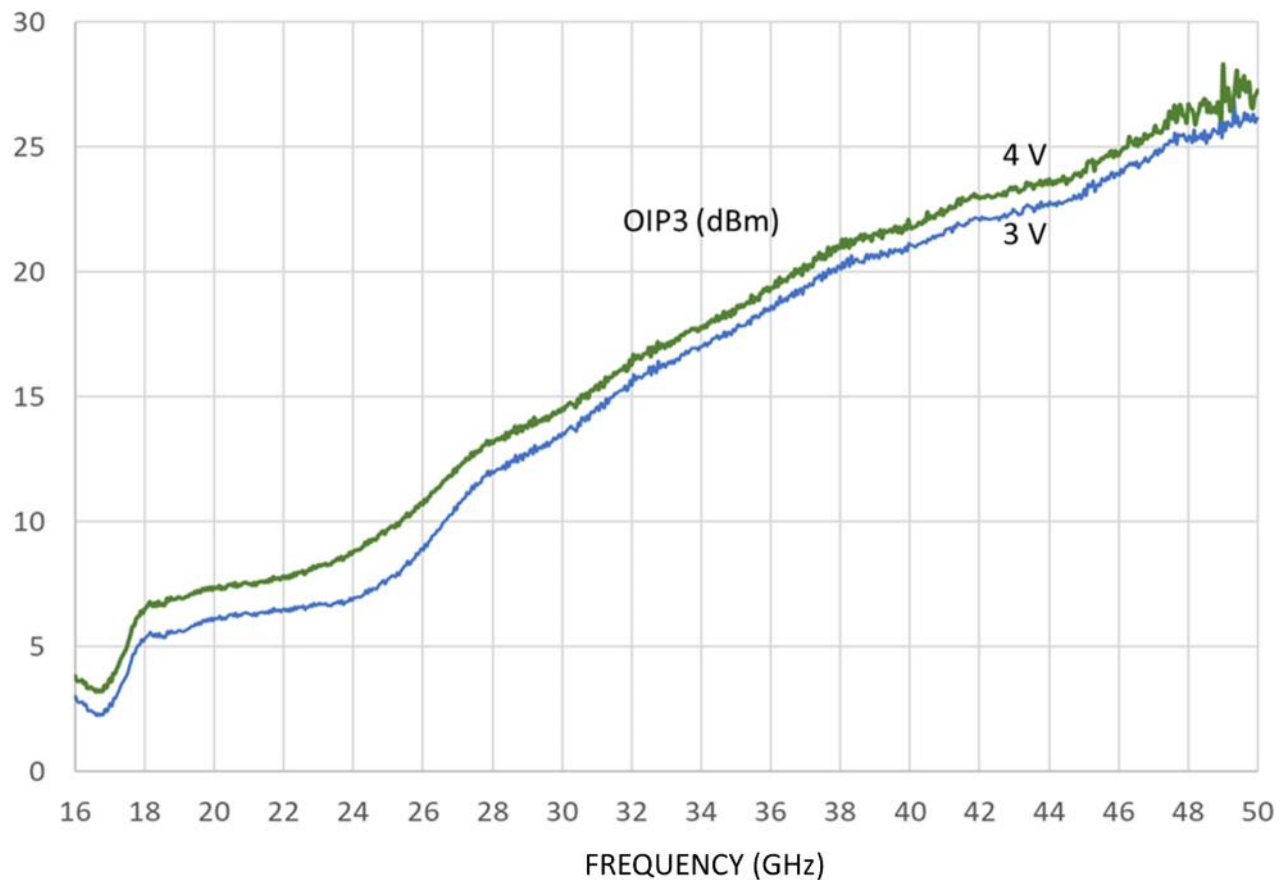
Measured Noise Figure, with wirebonds to external 50-ohm microstrip lines

VD = 3.0 V; ID = 72 mA; room temperature



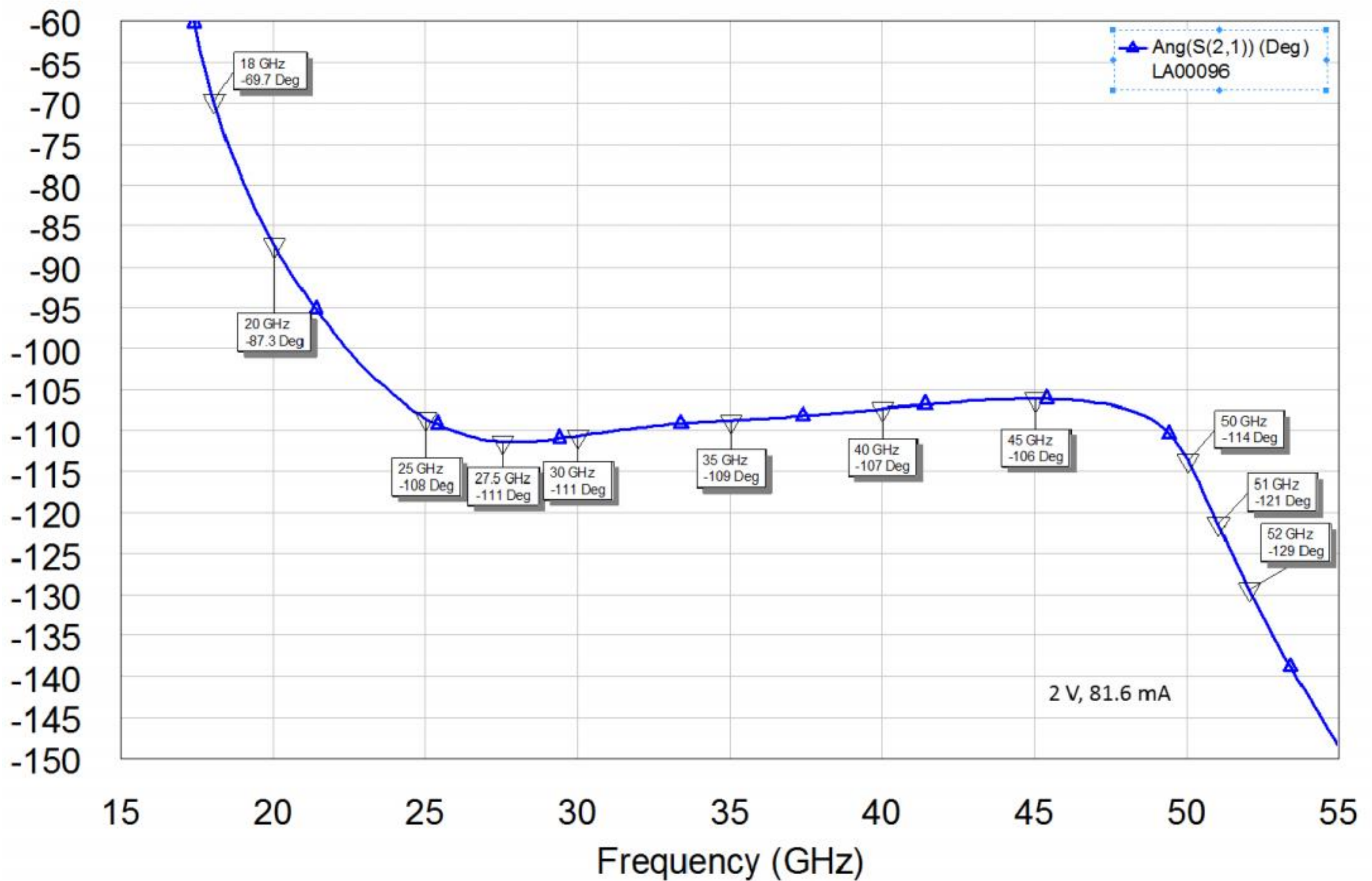
Measured Output Third-Order Intercept, with wirebonds to external 50-ohm microstrip lines

VD = 3.0 V; ID = 72 mA; room temperature; 10 MHz spacings; -20 dBm / tone

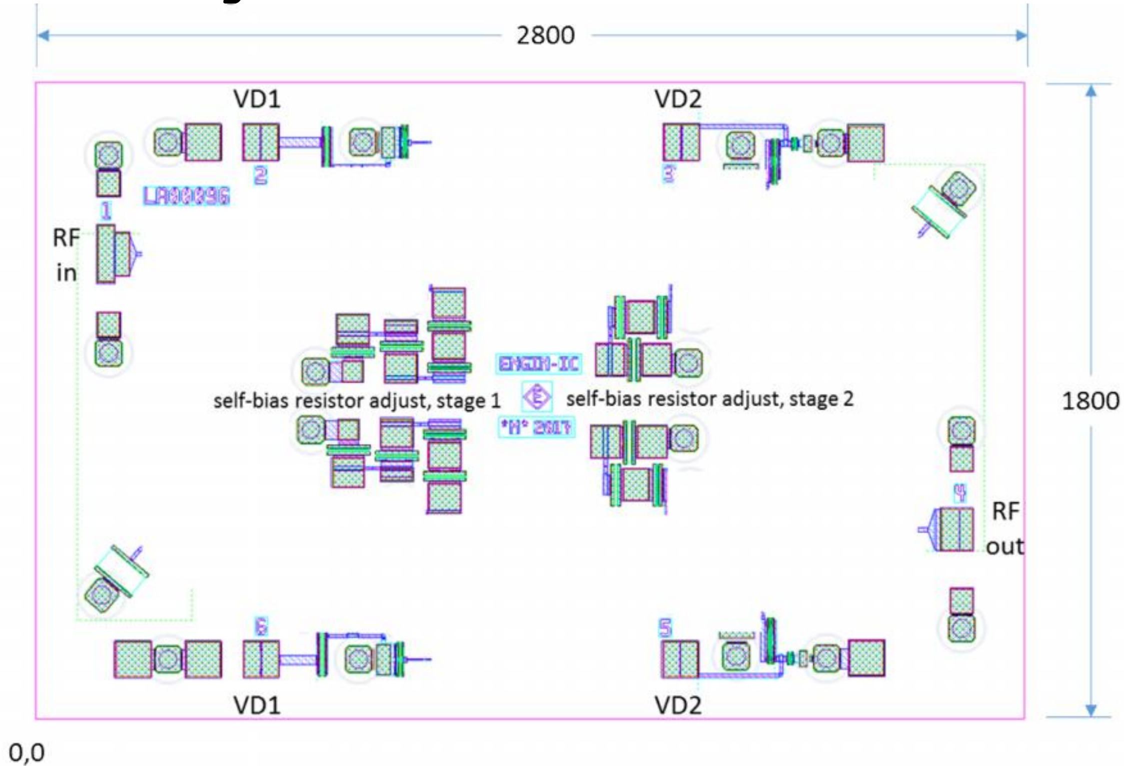


Predicted Deviation from Linear Phase (degrees), referenced to an ideal 50-ohm transmission line 240 degrees long at 10 GHz

VD = 2.0 V; ID = 81.6 mA; room temperature; linear model



Outline Drawing

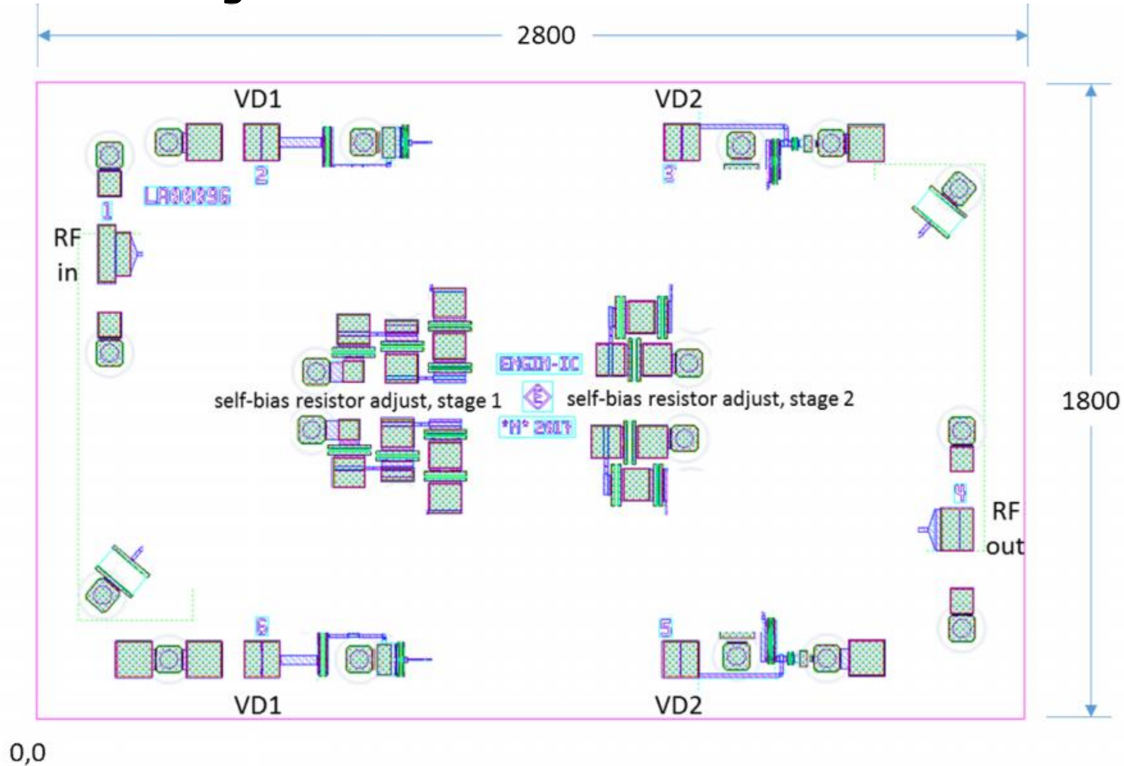


	Bond Pad Dimensions				
Pad	Description	Length	Width	Length	Width
		x-dim	y-dim	x-dim	y-dim
		(um)	(um)	(mils)	(mils)
1	RF input (port 1)	120	90	4.7	3.5
2	VD1 stage 1 upper	100	100	3.9	3.9
3	VD2 stage 2 upper	100	100	3.9	3.9
4	RF output (port 2)	120	90	4.7	3.5
5	VD2 stage 2 lower	100	100	3.9	3.9
6	VD1 stage 1 lower	100	100	3.9	3.9
	Self-bias adjust pads	75	75	3.0	3.0

Notes:

1. ***Pad dimensions are given in both µm and mils. Substrate thickness: 100 µm (0.004”).***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

Outline Drawing



	Bond Pad Center Point Locations				
Pad	Description	Length	Width	Length	Width
		x-dim	y-dim	x-dim	y-dim
		(um)	(um)	(mils)	(mils)
1	RF input (port 1)	224	1314	8.8	51.7
2	VD1 stage 1 upper	636	1630	25.0	64.2
3	VD2 stage 2 upper	1827	1630	71.9	64.2
4	RF output (port 2)	2607	536	102.6	21.1
5	VD2 stage 2 lower	1824	170	71.8	6.7
6	VD1 stage 1 lower	638	170	25.1	6.7

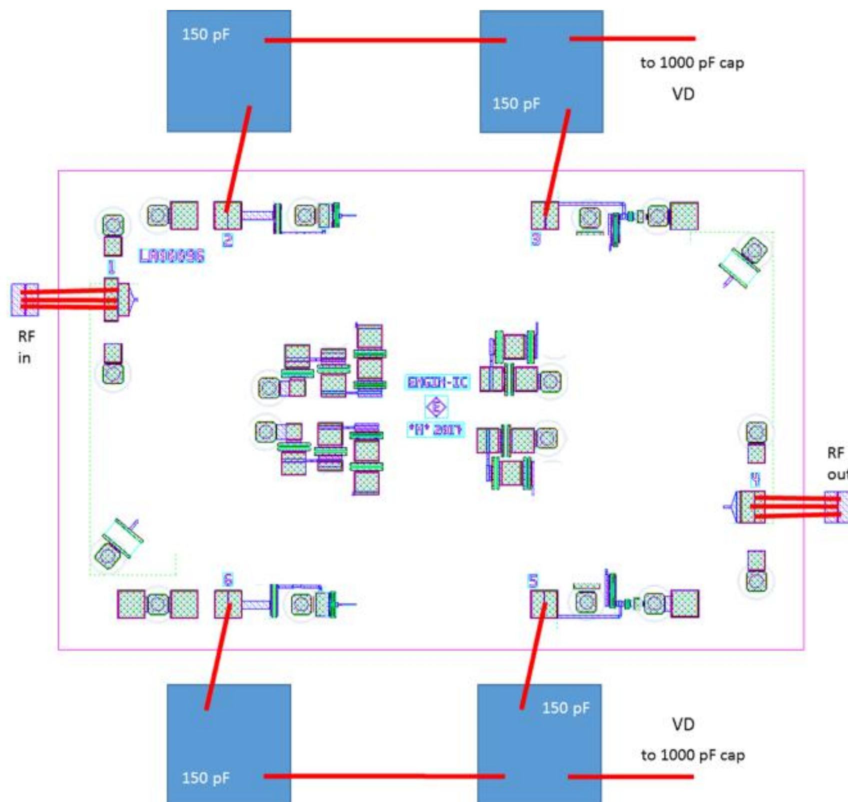
Notes:

1. ***Bond pad center locations are given in both µm and mils. GaAs Substrate thickness: 100 µm (0.004”).***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Flare Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level such that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).

	RF I/O - External Microstrip Flares on 5-mil Alumina					
	Flare	Flare	Wire	Wire	Wire	Number
Port	Length	Width	Inductance	Length	Length	of
	x-dim	y-dim				Wires
	(um)	(um)	(nH)	(um)	(mils)	
P1 RF input	no flare	120	0.065	254	10	3
P2 RF output	no flare	120	0.065	254	10	3
50-ohm line: 120 um wide on 5-mil alumina						



Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external flare to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
    - ***a) Diameter: 25.4 µm (1 mil); b) Spacing: 4 mils (~ 100 µm) typical***
    - ***c) Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)***
3. ***Wire Length is total length if the wire were made perfectly straight.***

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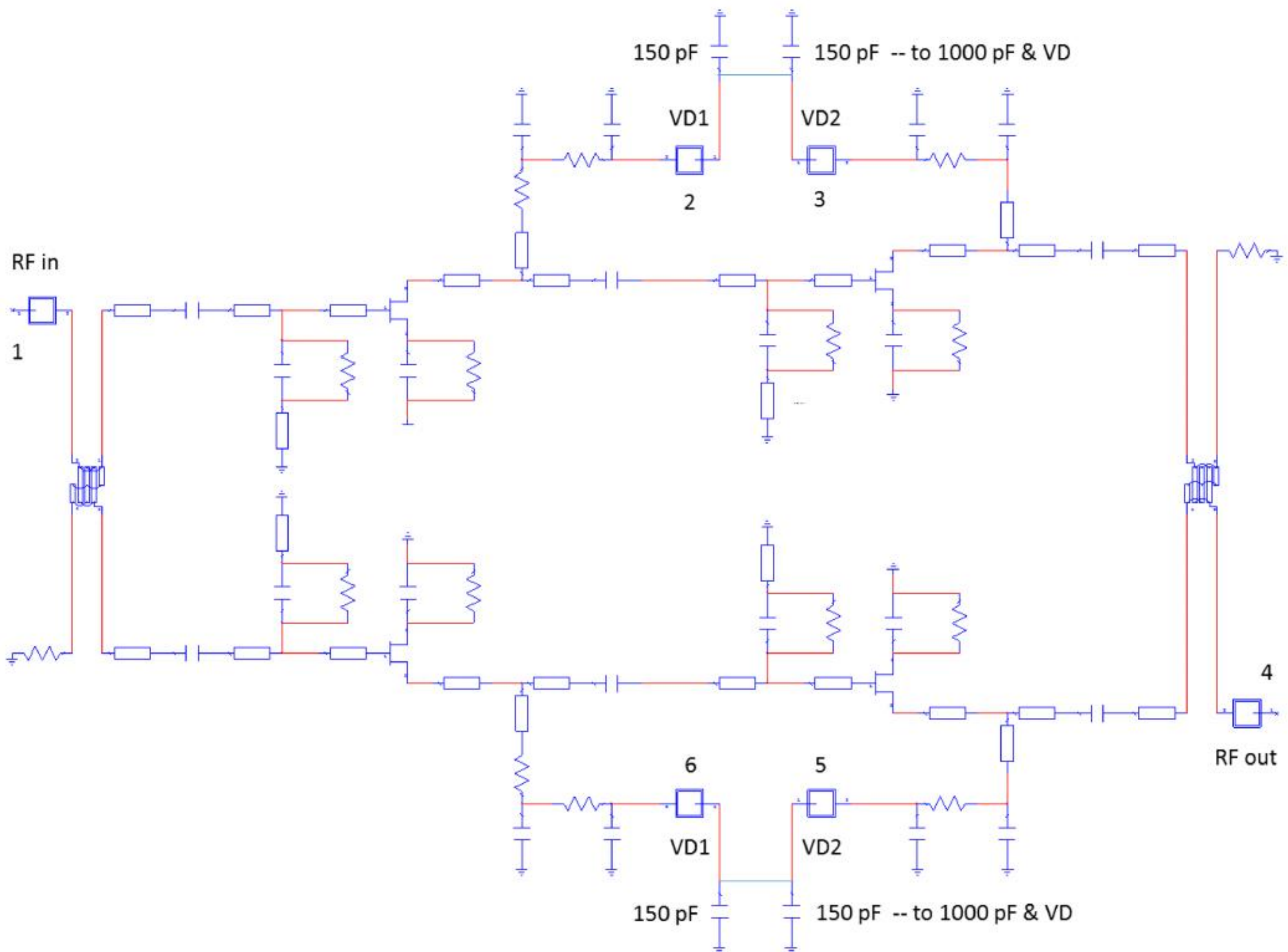
Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports high frequency performance. Care should be made to following the wirebond dimensions as shown in the flare diagram.

Application Circuit and Turn-on Procedure



Note 1: Internal blocking capacitors on RF in/out ports (P1 and P2).

Note 2: Performance is optimized for noise figure with VD set near 2.0 V. Output power at 1-dB gain compression can be increased by increasing VD to 3 or 4 V.