High Linearity Q-band LNA DIE, 43 to 50 GHz

ENGLA00111B

Typical Applications

- Military and Commercial SATCOM
- Obsolescence Replacement
- Receive or Transmit Circuits
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

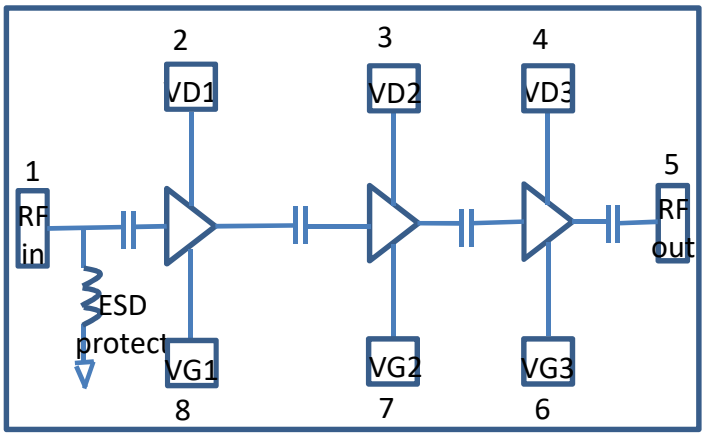
Features

- High gain 27– 30 dB
- Low noise figure 1.7 dB
- High linearity 23 dBm
- Good I/O return loss
  - 10 / 12 dB typical
- Multiple operating bias conditions
  - Low noise
  - High linearity
- Wide Vdd operating range 1 to 4.5 V
- On-chip input ESD protection
- Small size
  - 2.72 x 1.5 x 0.10 mm
  - 0.107 x 0.060 x 0.004 inch

Description

The ENGLA00111B is a high linearity Low-Noise Amplifier (LNA) operating across 43 to 50 GHz. The design is 50 ohm matched and includes on-board bias circuitry. The amplifier offers 30-dB gain; 1.7-dB de-embedded noise figure; and > 23-dBm output third-order intercept point (OIP3) across the band, at room temperature. The amplifier can be operated at drain voltages 1 V to 4.5 V with a wide range of drain currents depending on low-noise or high linearity application. The MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds to external 50 ohm microstrip lines for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



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Electrical Specifications, T = 25 ^{o}C, VD1= 2.3 V; VD2=2.3 V; VD3=4.3 V; ID total =65 mA VG1 = -0.14 V, ID1 = 14.5 mA, VG2 = -0.08 V, ID2 = 18.5 mA, VG3 = -0.06 V, ID3 = 32 mA

Parameter	Min	Typ	Max	Units
Frequency Range		43-50		GHz
Gain	26	28	30	dB
Noise Figure(1)		1.7	2.0	dB
Input Return Loss		10		dB
Output Return Loss		12		dB
Output P1dB		13		dBm
Output IP3 (Low Noise Bias)	22	23	25	dBm
Supply Current		65		mA
Thermal Resistance(2)		420		^{o}C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD	1.0	2.3	4.5	V
ID		65		mA
VG	-0.30	-0.14	-0.05	V

(1) NF De-embedded Input Loss

(2) Channel to MMIC Backside; Backside Temp is 80 ^{o}C

Absolute Maximum Ratings

Parameter	Max level
Drain Voltage, VD	5.0 V
Gate Voltage, VG	-2.0 V
RF Input Power	+17 dBm
Channel Temperature	+170 ^{o}C
Operating Temperature	-55 ^{o}C to +80 ^{o}C
Storage Temperature	-65 ^{o}C to +150 ^{o}C

LNA can be operated with common drain voltage for all 3 stages at 1 V to 4 V , keeping approximate gate voltages as shown below.

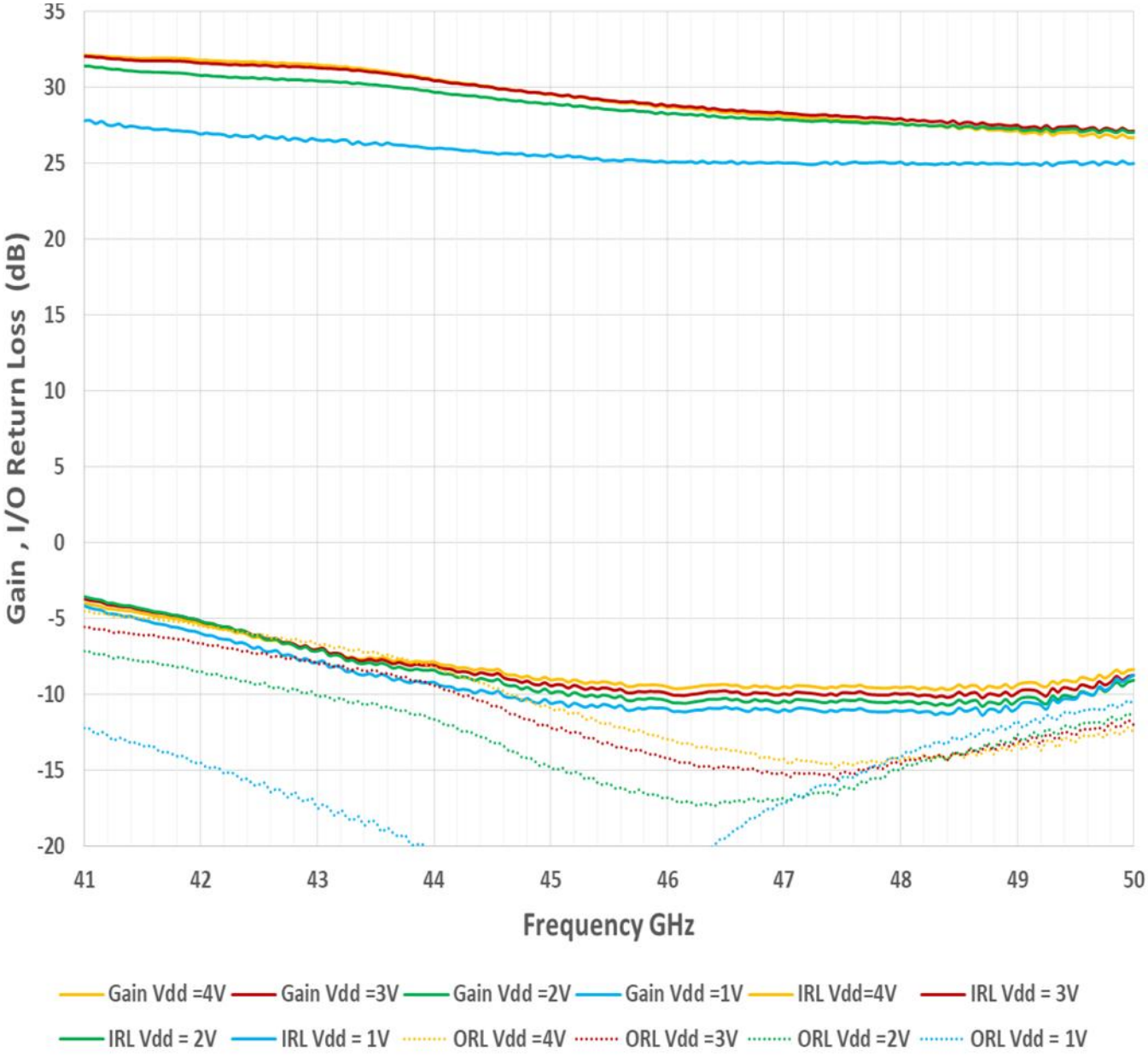
LA00111B is a versatile Q band LNA that can be operated at various bias conditions with various degrees of RF Performance: Low Noise, High Linearity, Low DC Power, etc., depending on the application requirement appropriate bias condition can be chosen.

Suitable for Low Voltage Q-band T / R modules.

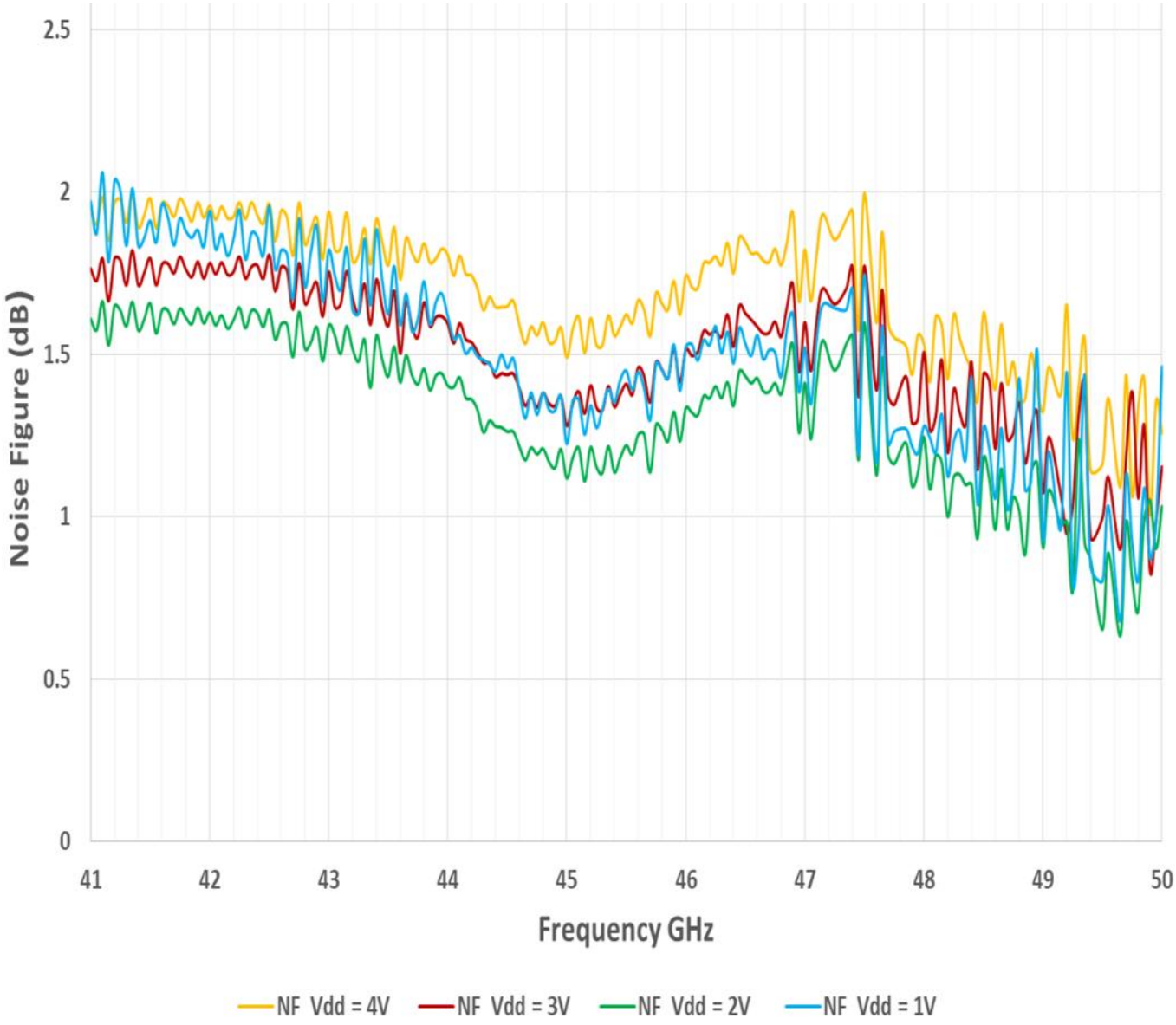
Following pages show Gain, I/O Return loss, Noise Figure and OIP3 at T = 25 ^{o}C at Vdd = 1 V to 4 V

	Vg1 = -0.14V	Vg2 = -0.08V	Vg3 = -0.06V	
Vdd	Idd1	Idd2	Idd3	Total Idd
V	mA	mA	mA	mA
1	9.6	13	16.3	38.9
2	13.6	17.5	21.3	52.4
3	17	21.3	25.5	63.8
4	20.3	25.1	30.9	76.3

Measured Gain and Input/Output Return Loss (dB), with wirebonds and external microstrip flare line at Vdd = 1 V to 4 V



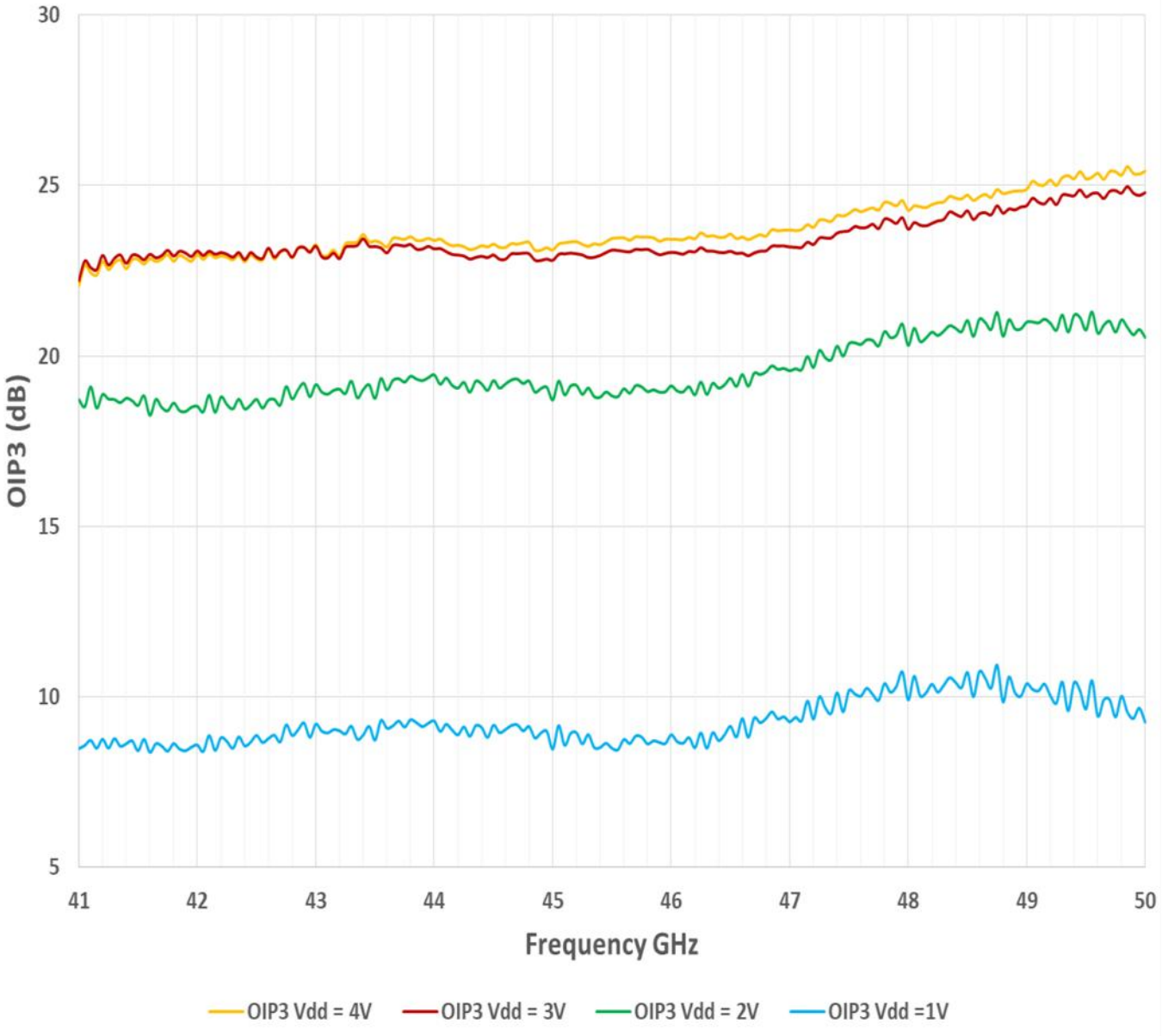
Measured Noise Figure (dB), with wirebonds and external microstrip flare line at Vdd = 1 V to 4 V



**** Noise Figure De-embedded Input Loss***

Measured Output Third-Order Intercept Point (OIP3, dBm), with wirebonds and external microstrip flare line at Vdd = 1 V to 4 V

RF input tone levels: -25 dBm per tone; tone spacing: 100 MHz



Measured Gain and Input/Output Return Loss (dB), with wirebonds and external microstrip flares

Nominal Low Noise Bias Condition

T = 25 ^{o}C, VD1 = 2.3 V; VD2 = 2.3 V; VD3 = 4.3 V; ID total = 65 mA

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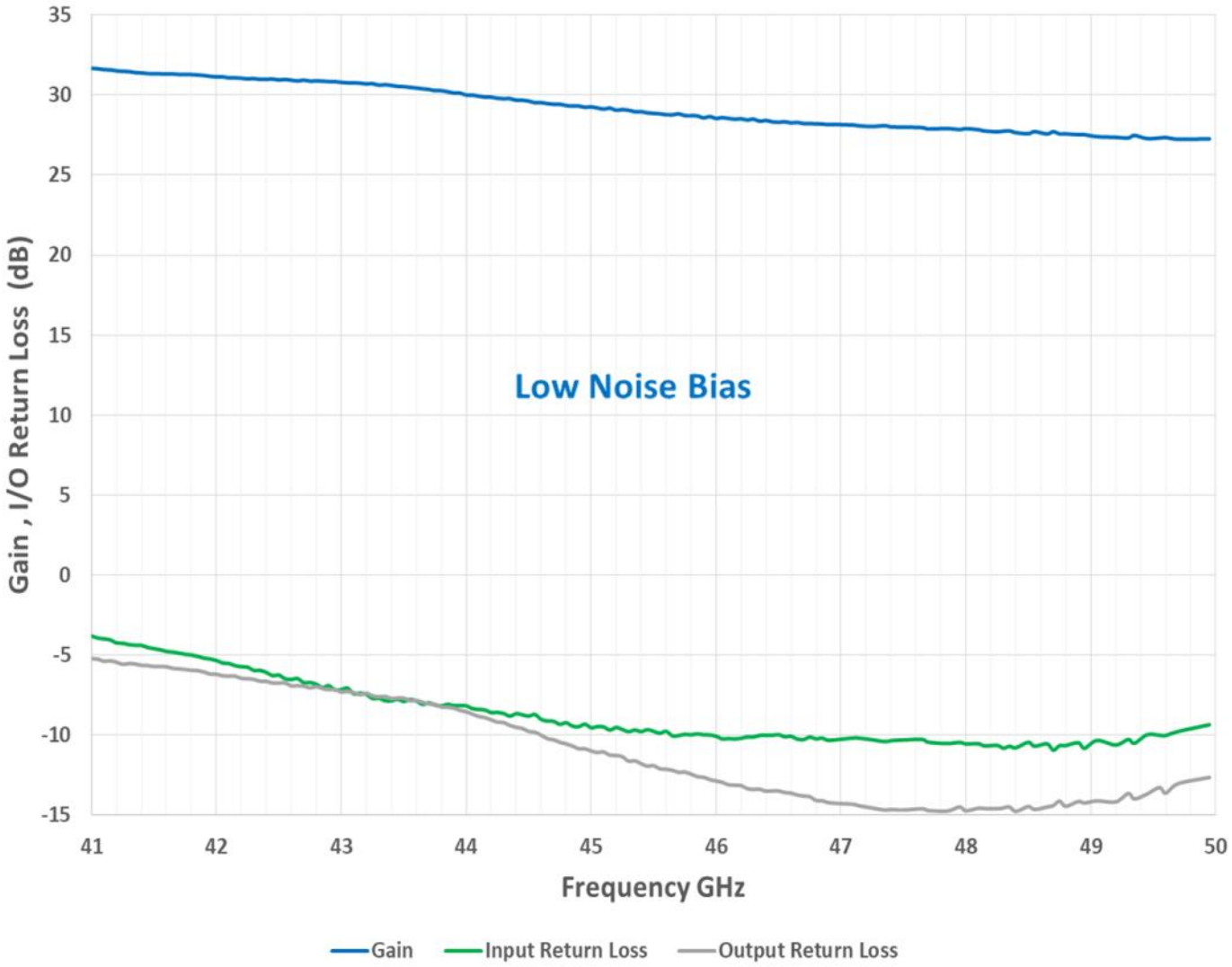

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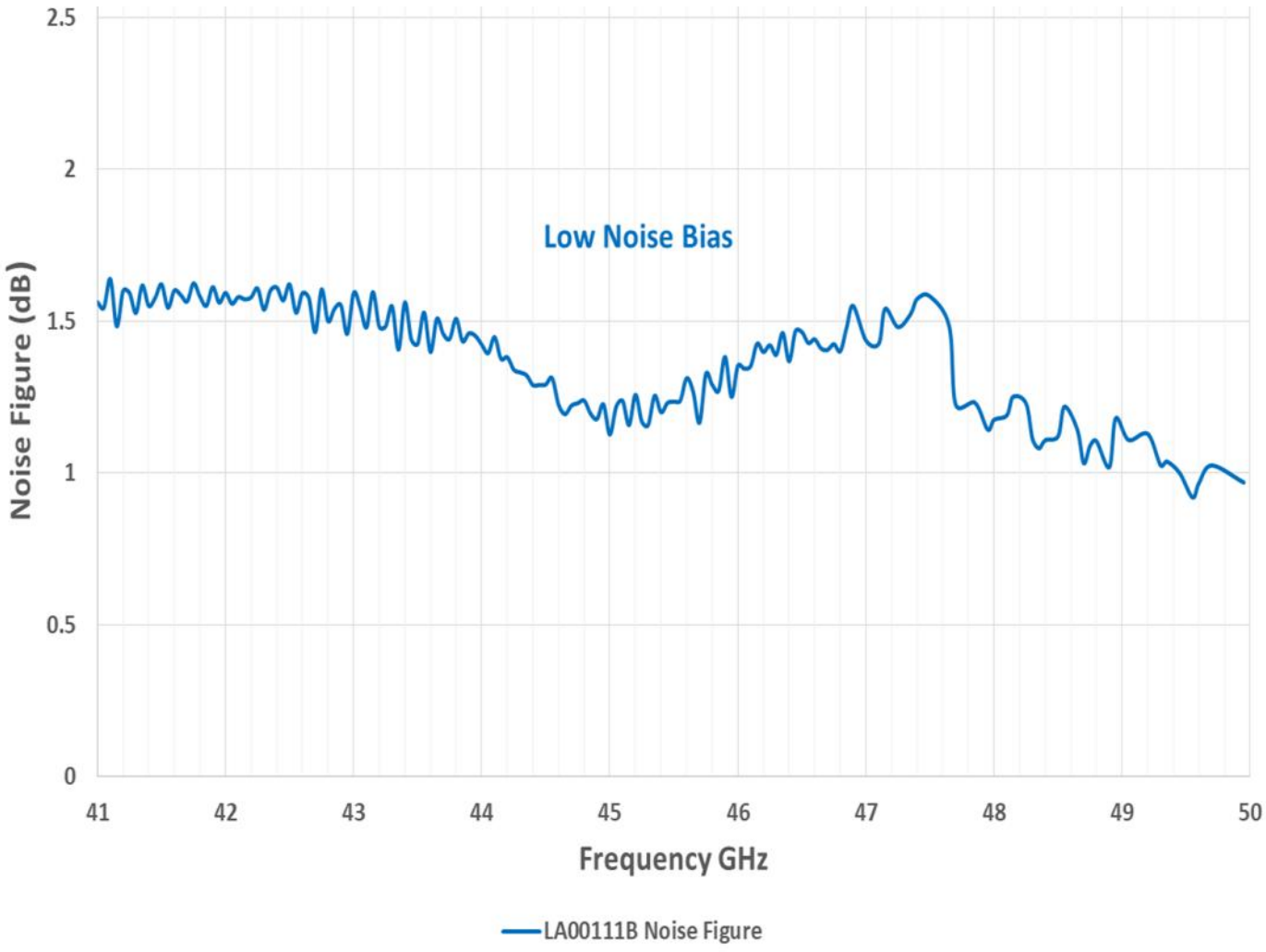

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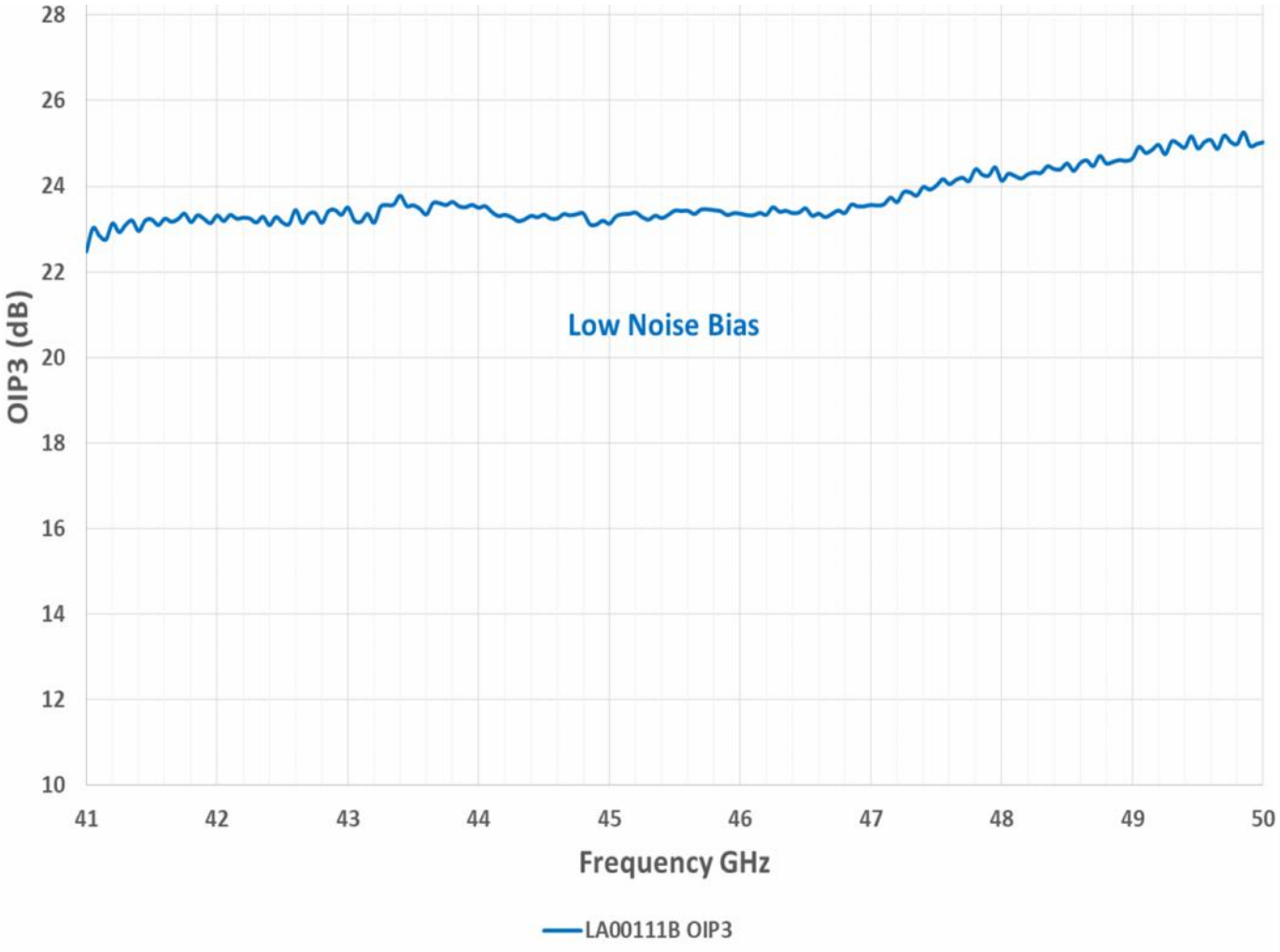
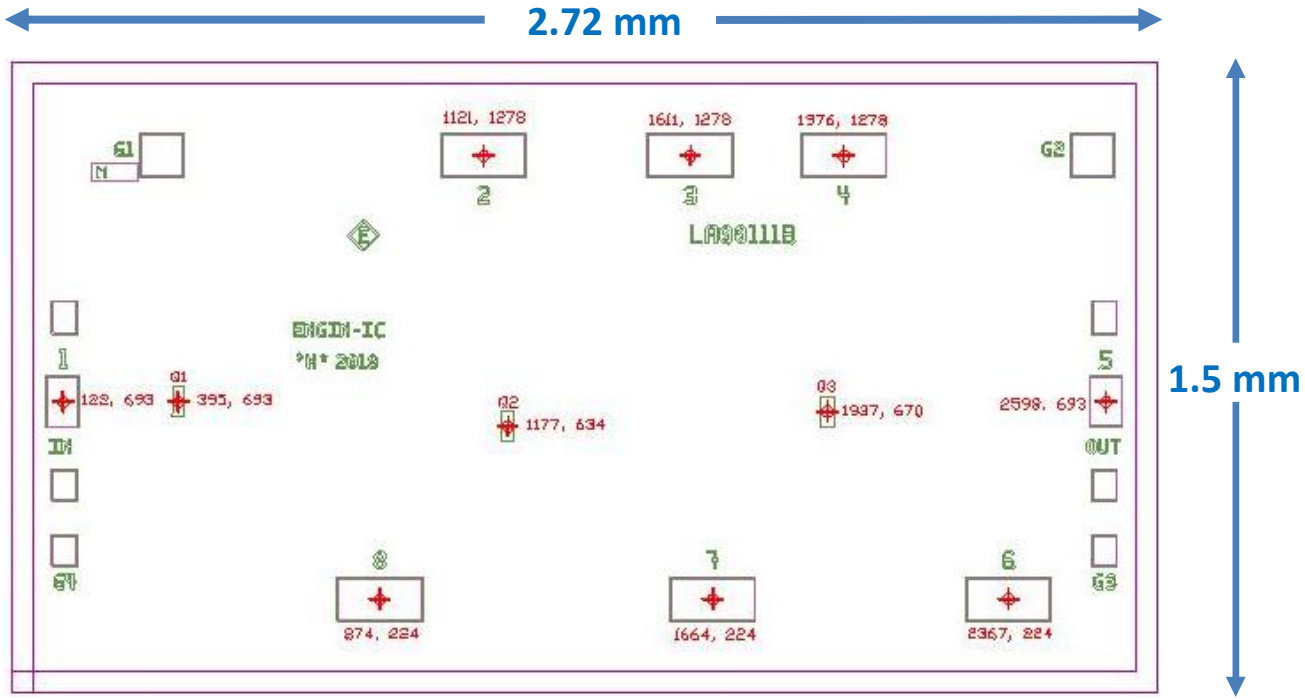


MMIC Outline & PAD Location Drawing



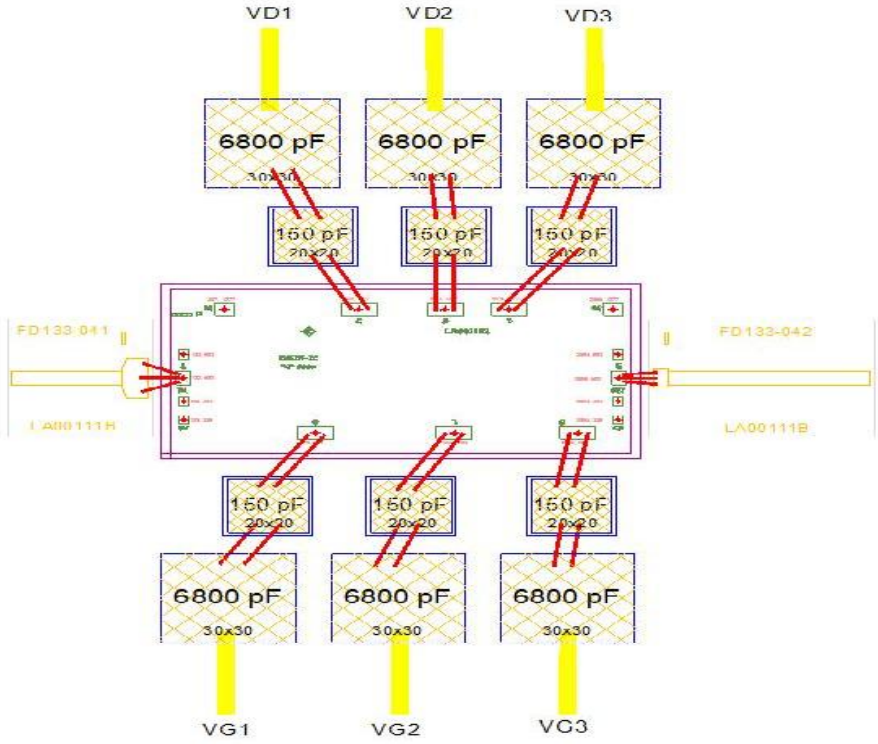
Pad	Description	Length x-dim (um)	Width y-dim (um)	Length x-dim (mils)	Width y-dim (mils)
1	RF input (port 1)	122	693	4.8	27.3
2	VD1 stage 1 drain bias	1121	1278	44.1	50.3
3	VD2 stage 2 drain bias	1611	1278	63.4	50.3
4	VD3 stage 3 drain bias	1976	1278	77.8	50.3
5	RF output (port 2)	2598	693	102.3	27.3
6	VG3 stage 3 gate bias	2367	224	93.2	8.8
7	VG2 stage 2 gate bias	1664	224	65.5	8.8
8	VG1 stage 1 gate bias	874	224	34.4	8.8

Notes:

1. ***Bond pad center locations are given in both µm and mils. Substrate thickness: 100 µm (0.004”).***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Line Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level so that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).



	RF I/O - External 50 ohm Microstrip Line on 5-mil Alumina					
	Flare	Flare	Wire	Wire	Wire	Number
Port	Length	Width	Inductance	Length	Length	of
	x-dim	y-dim				Wires
	(um)	(um)	(nH)	(um)	(mils)	
P1 RF input	124	338	0.115	230	9	3
P2 RF output	82.25	160	0.115	230	9	3
	50-ohm line					

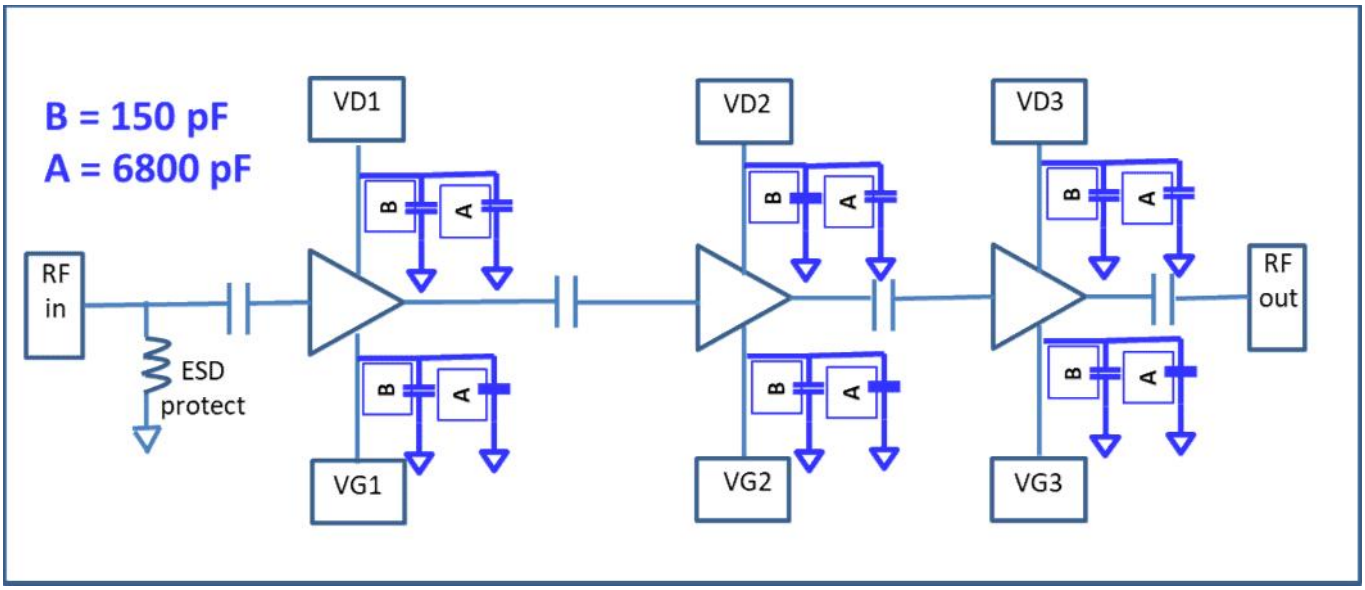
Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external 50 ohm line to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
   - ***a) Diameter: 25.4 µm (1 mil); b) Spacing: 4 mils (~ 100 µm) typical***
   - ***c) Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)***
3. ***Wire Length is total length if the wire were made perfectly straight.***

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports broadband performance . Follow the wirebond dimensions as shown page7 flare diagram for optimum broadband I/O return loss.

Application Circuit and Turn-on Procedure



Note : VD1, VD2, VD3 can be combined after bypass capacitors for common voltage operation

Bias Up Sequence:

1. Set Idd limit to 100 mA
2. Set Gate Voltage (VG) = -2.0 V
3. Set Drain Voltages (VD) = 2.3, 2.3, 4.3 V (higher OIP3), or 2.3 V, all stages
4. Adjust VG1, VG2, VG3 more positive until target ID1, ID2, ID3
5. Turn ON RF Signal

Bias Down Sequence:

1. Turn OFF RF Signal
2. Reduce VG to -2.0 V , Idd should be 0 mA
3. Reduce VD to 0 V
4. Turn OFF DC Supplies