Wideband Low DC Power LNA DIE, 2 to 18 GHz

ENGLA00182A

Typical Applications

- Military and Commercial SATCOM
- Obsolescence Replacement
- Receive or Transmit Circuits
- Telecom Infrastructure
- Space Hybrids
- Test and Measurement Systems

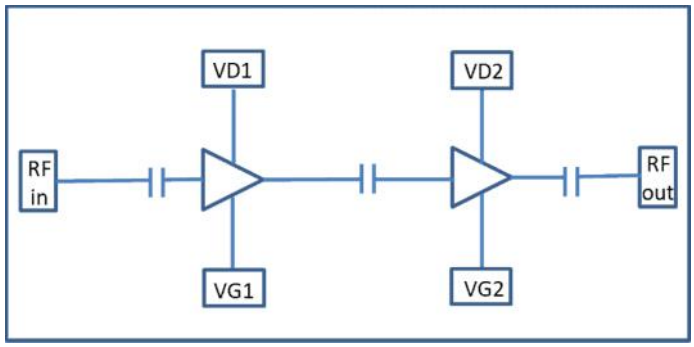
Features

- LOW DC Power
  - 40 mW @ Vd1 =1.5 V
  - 132 mW @ Vd1 =3.3 V
- Gain 15 – 17.5 dB
- Low Noise Figure -- 2.0 dB
- Multiple Operating Bias Conditions
  - Low DC Power
  - Low Noise
- Good I/O return loss
  - 10 / 15 dB typical
- Size
  - 2.72 x 1.65 x 0.10 mm
  - 0.107 x 0.065 x 0.004 inch

Description

The ENGLA00182A is a wideband low DC power low-noise Amplifier (LNA) operating across 2 to 18 GHz with only 40 mA DC current at Vdd = 3.3 V. The amplifier offers 17.5-dB gain, 2.0-dB de-embedded noise figure, and >18-dBm output third-order intercept point (OIP3) across the band, at room temperature. The design is 50 ohm matched and includes on board bias circuitry. The MMIC has gold backside metallization and is designed to be silver epoxy or gold-tin solder attached. The RF interconnects are designed to account for wire bonds to external 50 ohm microstrip lines for optimal integrated return loss. No additional ground interconnects are required.

Functional Block Diagram



Electrical Specifications, T = 25 °C,
VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA

Parameter	Min	Typ	Max	Units
Frequency Range		2.0 – 18		GHz
Gain	15	17.5	18	dB
Noise Figure(1)		2.0	3.0	dB
Input Return Loss		10		dB
Output Return Loss		>15 below 12 GHz 10 above 12 GHz		dB
Output P1dB		12		dBm
Output IP3	18	22		dBm
Supply Current		40		mA
Thermal Resistance(2)		136		°C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD	1.5	3.3	4.0	V
ID		40		mA
VG	-0.3	-0.17	+1.0	V

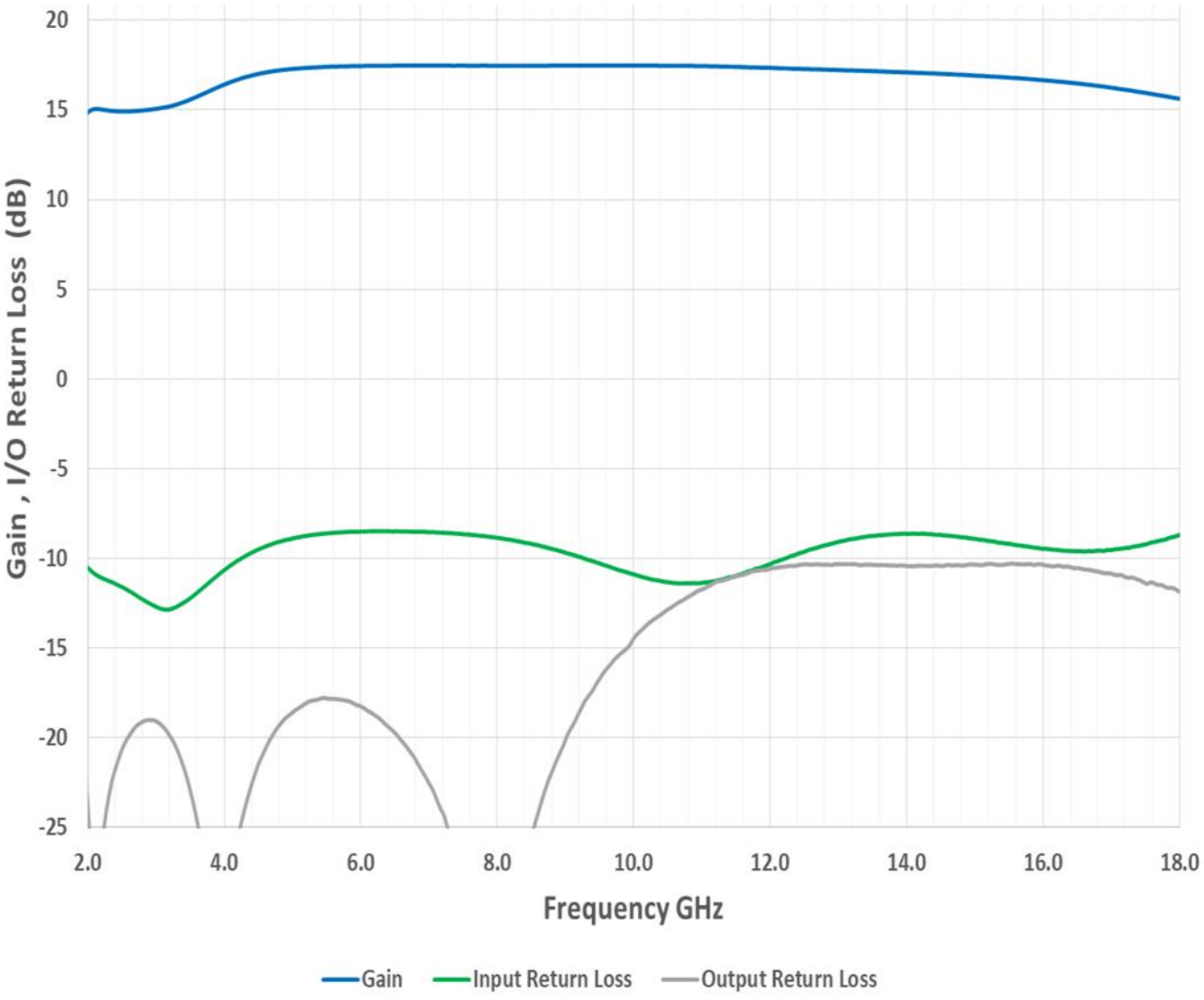
(1) NF De-embedded Input Loss
(2) Channel to MMIC Backside; Backside Temp is 100 °C

Absolute Maximum Ratings

Parameter	Max level
Drain Voltage, VD	5.0 V
Gate Voltage, VG	-2.5 V / + 1.5 V
RF Input Power	+17 dBm
Channel Temperature	+170 °C
Operating Temperature	-55 °C to +100 °C
Storage Temperature	-65 °C to +150 °C

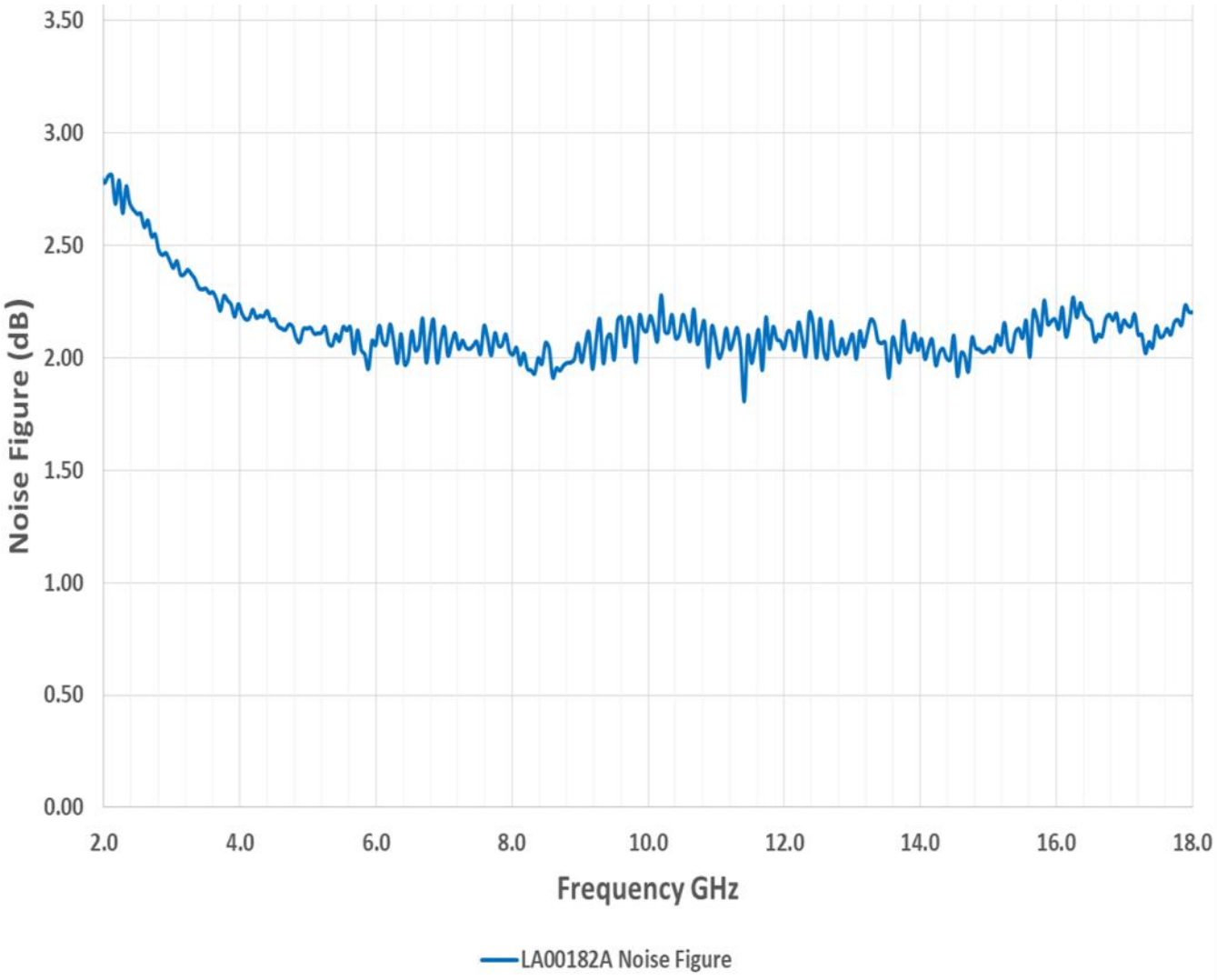
Measured Gain and Input/Output Return Loss (dB), with wirebonds and external microstrip flare line

T = 25 ^{o}C, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA



Measured Noise Figure (dB), with wirebonds and external microstrip flare line

T = 25 ^{o}C, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA

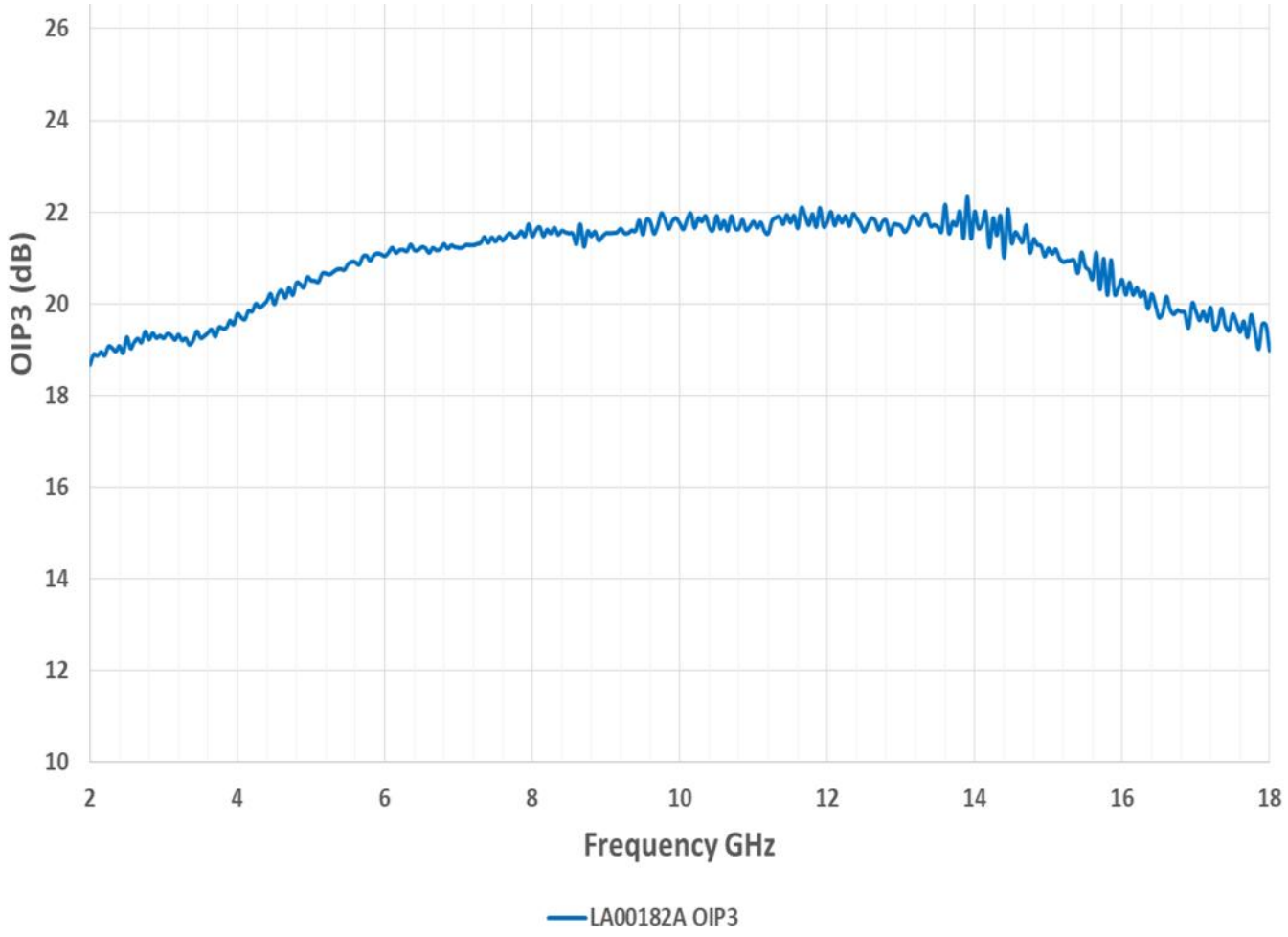


**** Noise Figure De-embedded Input Loss***

Measured Output Third-Order Intercept Point (OIP3, dBm), with wirebonds and external microstrip flare line

T = 25 ^{o}C, VD1 = 3.3 V; VG1 = +1.0 V; VG2 = -0.17 V; IDD = 40 mA

RF input tone levels: -25 dBm per tone ; tone spacing: 100 MHz



LNA can be operated with single drain voltage in the range of 1.5 V to 4 V

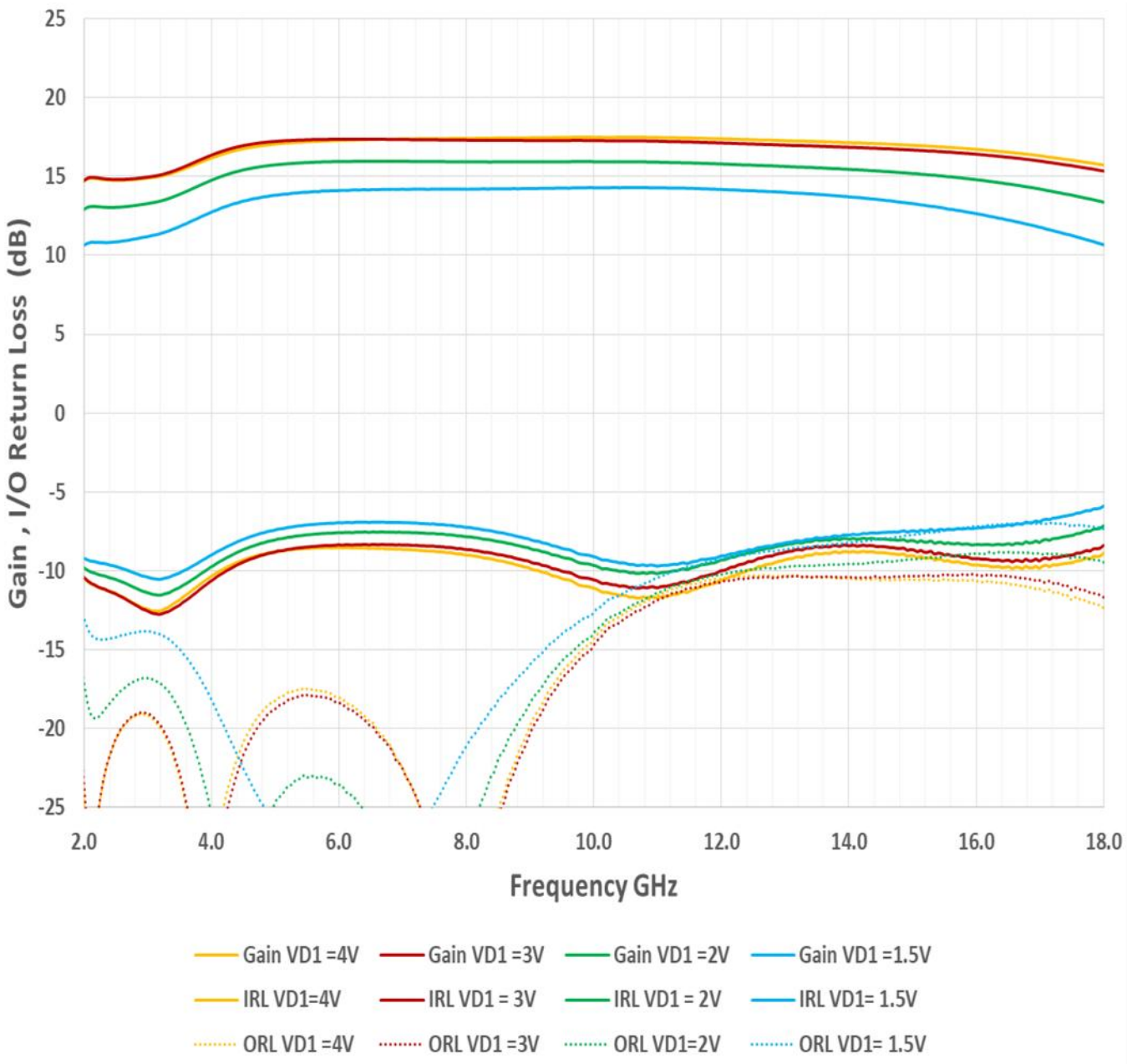
LA00182A is a versatile Wideband Low DC Power LNA that can be operated at various bias conditions with various degrees of RF Performance: Low Noise or Low DC Power and depending on the application requirement appropriate bias condition can be chosen.

Suitable for Low Power T / R Modules

Following pages show Gain, I/O Return loss, Noise Figure and OIP3 at T = 25 ^{o}C at Vdd = 1.5 V to 4 V

VD1	VG1	VG2	IDD
V	V	V	mA
1.5	+0.25	-0.17	27
2	+0.5	-0.17	32
3	+1.0	-0.17	40
4	+1.0	-0.17	41

Measured Gain and Input/Output Return Loss (dB), with wirebonds and external microstrip flare line at Vdd = 1.5 V to 4 V

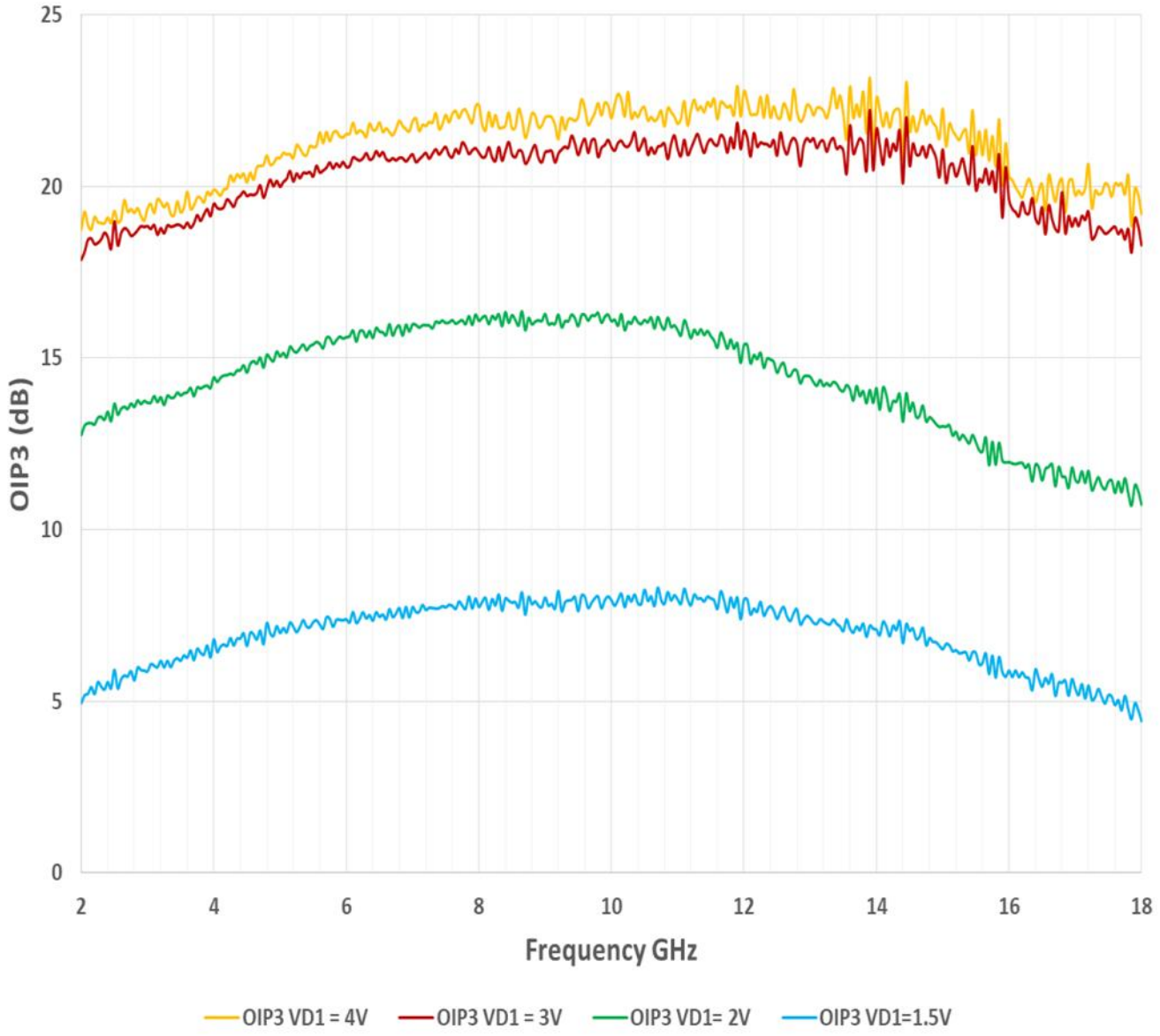


Measured Noise Figure (dB), with wirebonds and external microstrip flare line at Vdd = 1.5 V to 4 V

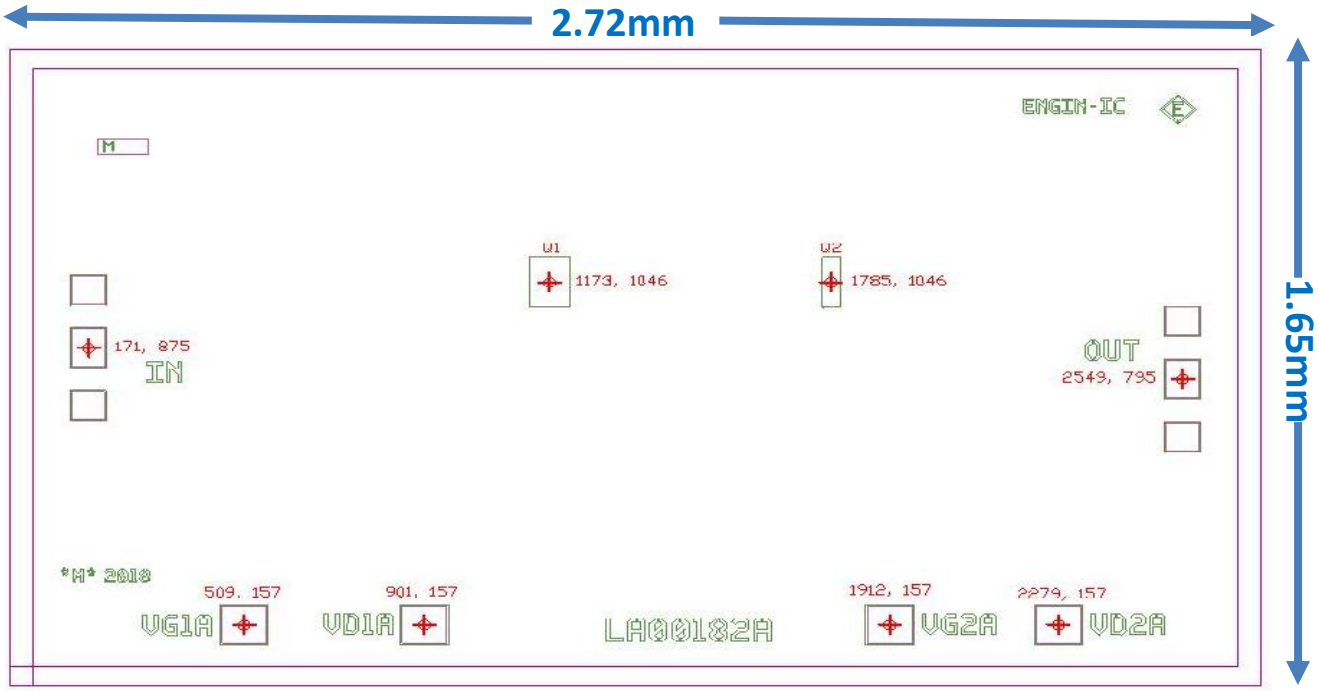
**** Noise Figure De-embedded Input Loss***

Measured Output Third-Order Intercept Point (OIP3, dBm), with wirebonds and external microstrip flare line at Vdd = 1.5 V to 4 V

RF input tone levels: -25 dBm per tone; tone spacing: 100 MHz



MMIC Outline & PAD Location Drawing



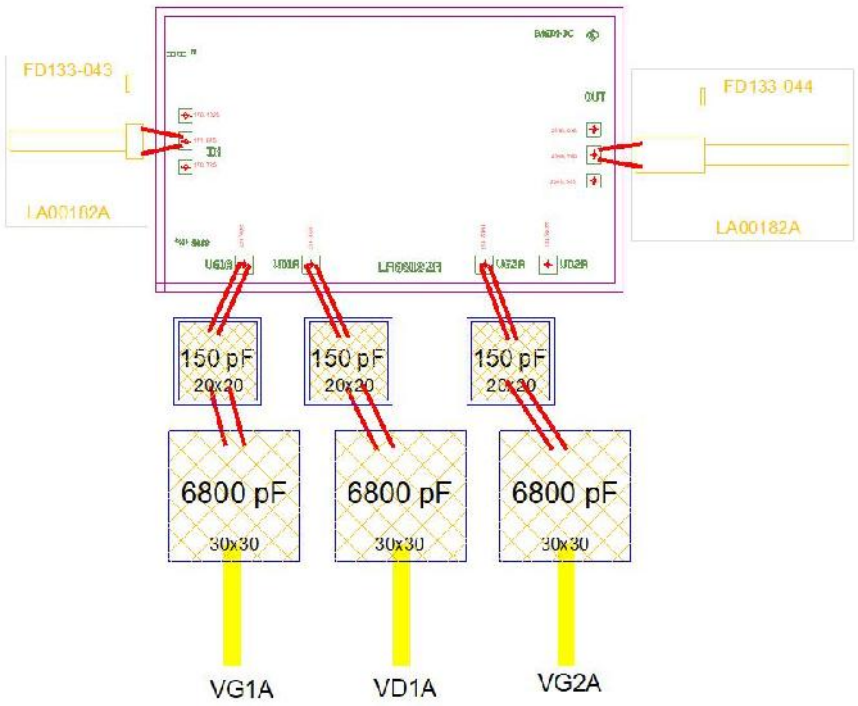
	Bond Pad Center Point Locations				
Pad	Description	Length	Width	Length	Width
		x-dim	y-dim	x-dim	y-dim
		(um)	(um)	(mils)	(mils)
IN	RF input (port 1)	171	875	6.7	34.4
VG1A	VG1 stage 1 gate bias	509	157	20.0	6.2
VD1A	VD1 stage 1 drain bias	901	157	35.5	6.2
VG2A	VG2 stage 2 gate bias	1912	157	75.3	6.2
VD2A	VD2 No Connect	2279	157	89.7	6.2
OUT	RF output (port 2)	2549	795	100.4	31.3

Notes:

1. ***Bond pad center locations are given in both µm and mils. Substrate thickness: 100 µm (0.004").***
2. ***Backside metallization is gold.***
3. ***Bond pad metallization is gold.***

External I/O Microstrip Line Dimensions (on 5-mil Alumina) and I/O Bond Wire Inductances for Optimum Insertion and Return Loss Performance

S-parameters can be supplied at DIE level so that optimal flare dimensions can be made for the substrate connection medium used (if different from 5-mil Alumina).



	RF I/O - External 50 ohm Microstrip Line on 5-mil Alumina					
	Flare	Flare	Wire	Wire	Wire	Number
Port	Length	Width	Inductance	Length	Length	of
	x-dim	y-dim				Wires
	(um)	(um)	(nH)	(um)	(mils)	
P1 RF input	100	200	0.115	230	9	2
P2 RF output	394	204	0.115	230	9	2
	50-ohm line					

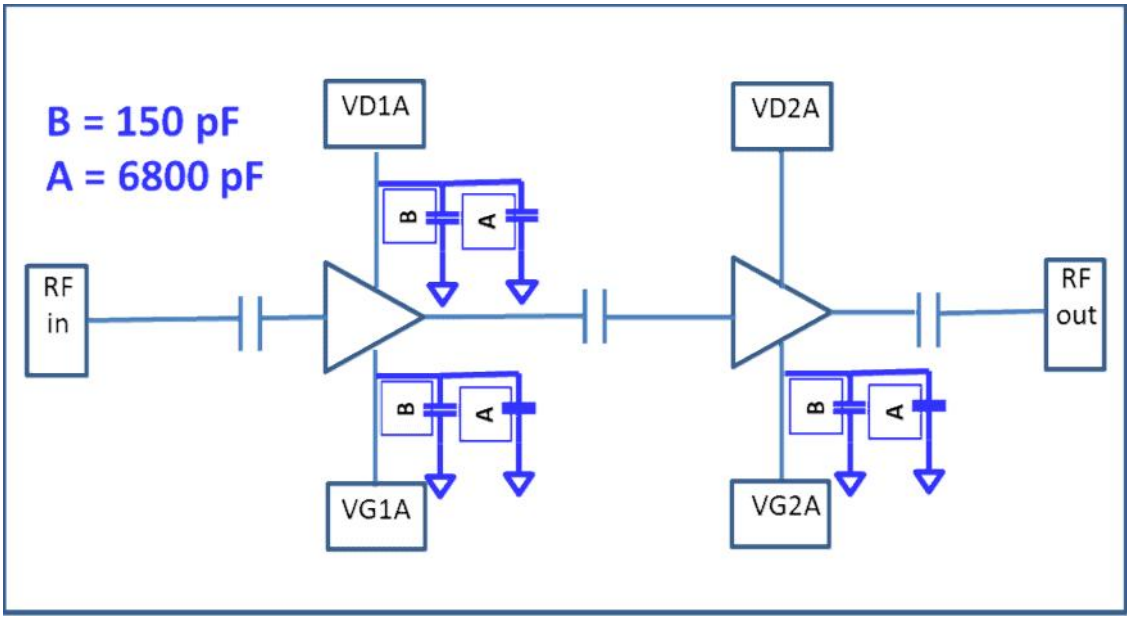
Notes:

1. ***To achieve bond wire inductance noted, bond the number of wires shown in parallel from each external 50 ohm line to each associated MMIC RF bond pad as shown above.***
2. ***Gold Wire details:***
   - ***a) Diameter: 25.4 µm (1 mil); b) Spacing: 4 mils (~ 100 µm) typical***
   - ***c) Height above Ground: 8 mils (~ 200 µm) typical (wedge bonds)***
3. ***Wire Length is total length if the wire were made perfectly straight.***

Assembly Guidelines

The backside metallization is RF/DC ground. Attachment should be accomplished with electrically and thermally conductive epoxy, or with gold-tin (AuSn) solder. This device supports broadband performance . Follow the wirebond dimensions as shown page7 flare diagram for optimum broadband I/O return loss.

Application Circuit and Turn-on Procedure



Note : VD2A DO NOT CONNECT

Bias Up Sequence :

1. Set Idd limit to 50mA
2. Set Gate Voltage (VG) = -2.0 V
3. Set Drain Voltage (VD) = 3.3 V
4. Adjust VG2 more positive until target current , then adjust VG1 specified in page 2
5. Turn ON RF Signal

Bias Down Sequence :

1. Turn OFF RF Signal
2. Reduce VG to -2.0 V , Idd should be 0 mA
3. Reduce VD to 0 V
4. Turn OFF DC Supplies